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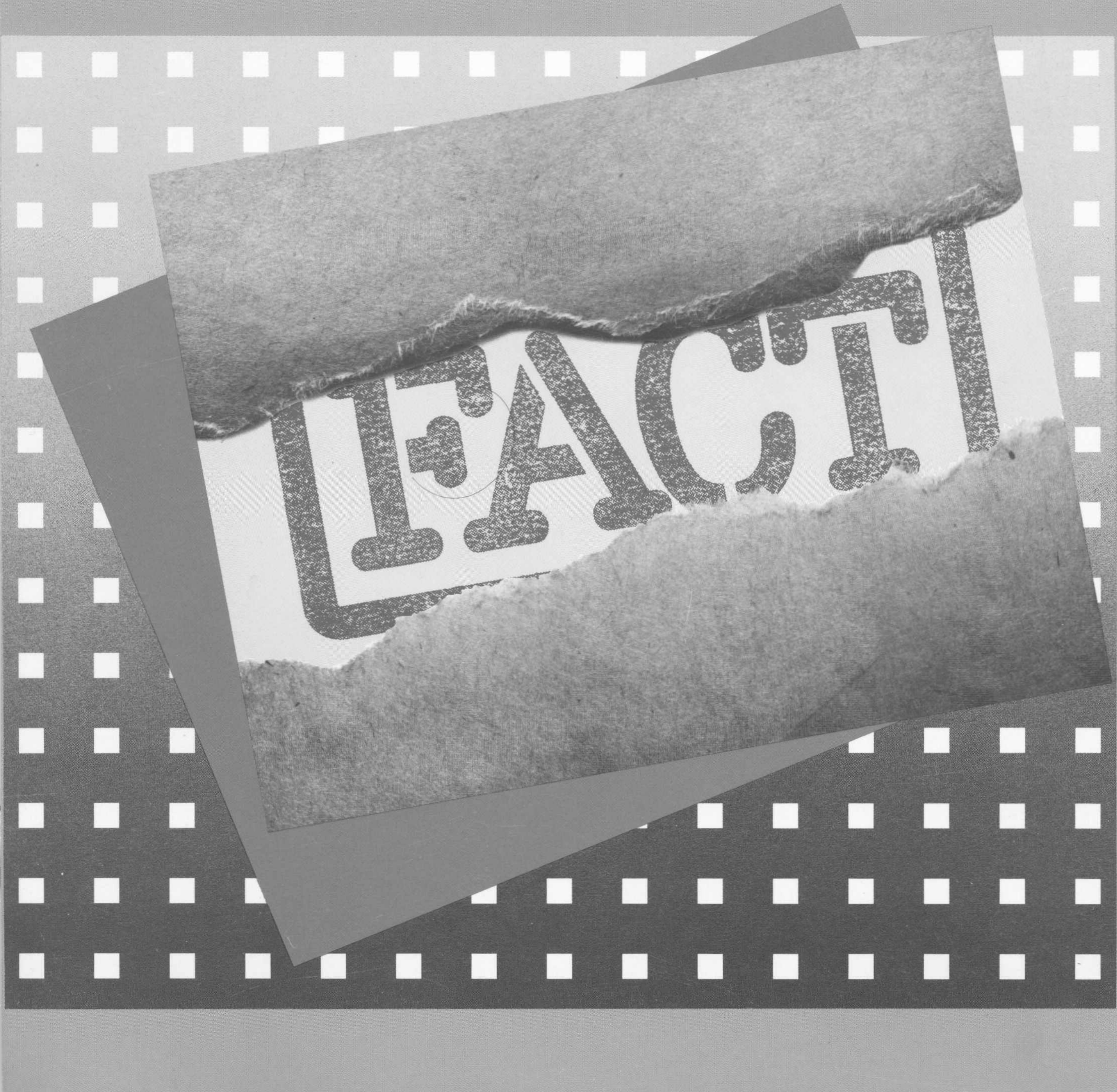
FACT

Fairchild Advanced CMOS Technology

Technology Seminar



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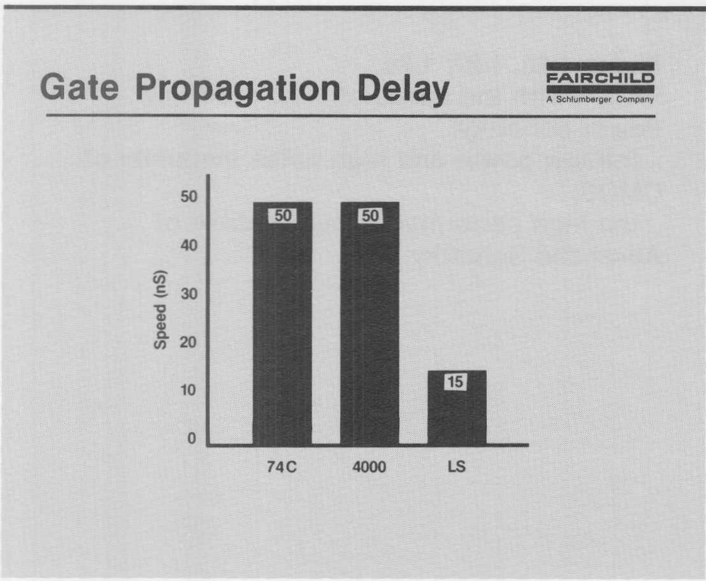
History



Slide 1.18
First in CMOS logic came the 4000 series, offering an extended operating voltage range. Then followed the 74C series. Both of these device families were also reliable. But, what the 74C and 4000 series gained in reliability they lost in speed.

Process

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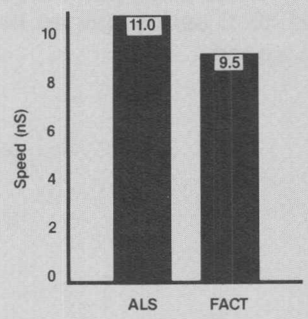
Gate Propagation Delay



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CMOS Technology

Power	5uW/Gate
Noise Margin (High/Low)	1.25/1.25 Volts

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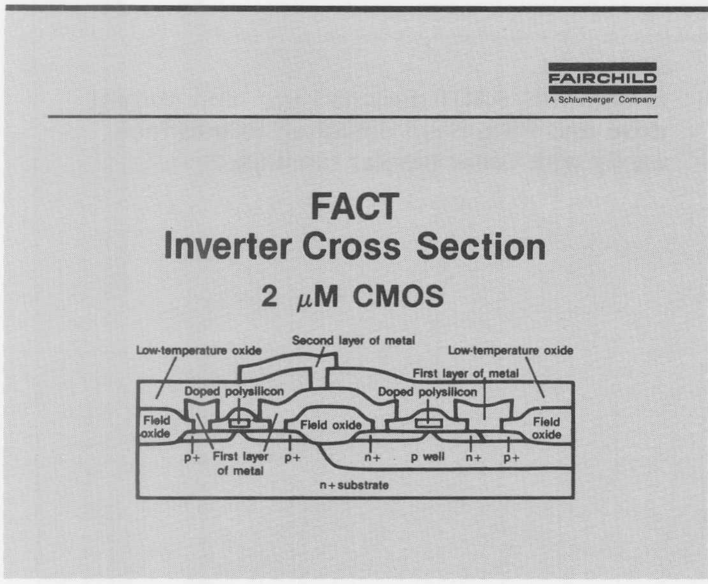
Output Drive

	I_{OH}	I_{OL}
FACT	- 24 mA	24 mA
AS/FAST	- 1.0 mA	20 mA

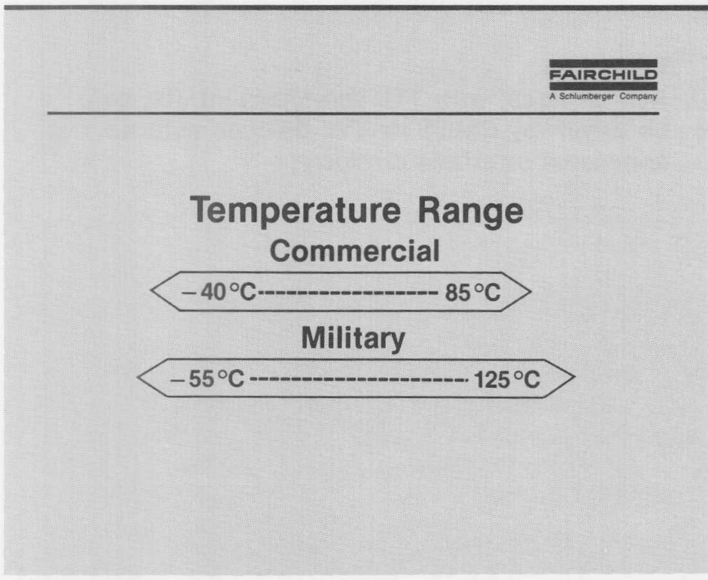
Slides 1.26, 1.27, 1.28
FACT...with the speed of Advanced Low Power Schottky;
...the low power and high noise immunity of CMOS;
...the high performance output drive of Advanced Schottky.

Process



Slide 1.32
As a result of our state-of-the-art sub 2 micron silicon gate process, FACT also facilitates a natural progression into state-of-the-art LSI density products.

Characteristics Overview



Slide 1.33A
FACT devices have been tested and are guaranteed to have an operating voltage range between 2 and 6 volts. They also operate with ambient temperatures of −40 to +85°C for the commercial temperature range and −55 to +125°C for the military temperature range.

Characteristics Overview

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FACT
Output Drive

I_{OH}/I_{OL} Static ± 24 mA
I_{OH}/I_{OL} Dynamic −75/+86 mA

Specifications are @ −40° to +85°C

Slide 1.34
In addition, FACT devices have high current drive and have been designed to interface easily with other bipolar families.

Characteristics Overview

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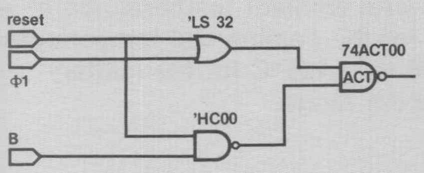

ACT Logic Interfaces with MOS and Bipolar Technologies

Slide 1.36
ACT devices, with TTL threshold inputs, can be driven by CMOS or TTL devices with no additional interface circuitry.

Characteristics Overview

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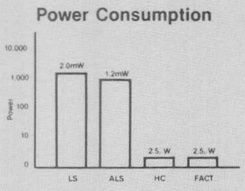

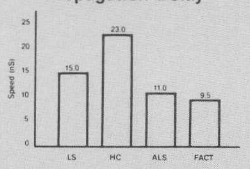

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Static Output Drive

	I_{OH}/I_{OL}
FACT	−24/24mA
ALS	−0.4/8mA
HC	−4mA/4mA

Dynamic Output Drive

	I_{OH_D}/I_{OL_D}
FACT	−75/86mA
ALS	Not Specified
HC	Not Specified
LS	Not Specified

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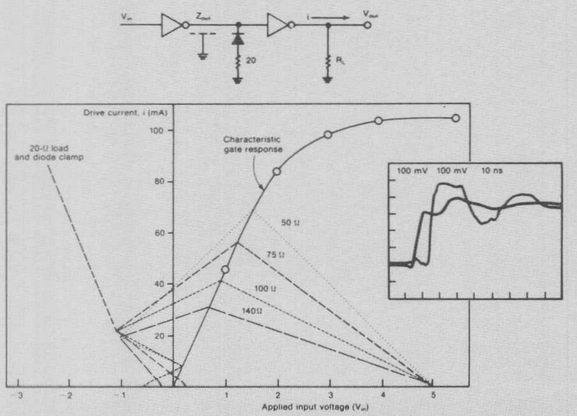

Slides 1.37, 1.37A, 1.38
When put to the test, FACT far outperforms LS, ALS and HC in speed, power and dynamic as well as static output drive. FACT's internal gate delays are more than twice as fast as LS devices. Incident wave switching on 50 ohm transmission lines is superior to all competitors. FACT offers output impedance that is lower than either ALS or HC. And, if LS TTL devices are replaced with FACT, operating currents may typically drop by more than 600 milliamps in a system application.

Characteristics Overview

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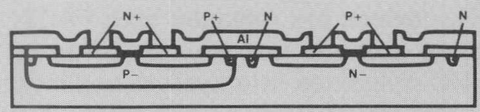
74C/4000 Type Inverter Cross Section

5-6 μM CMOS



FAIRCHILD
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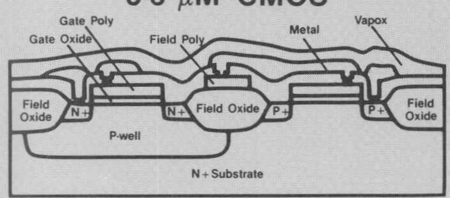
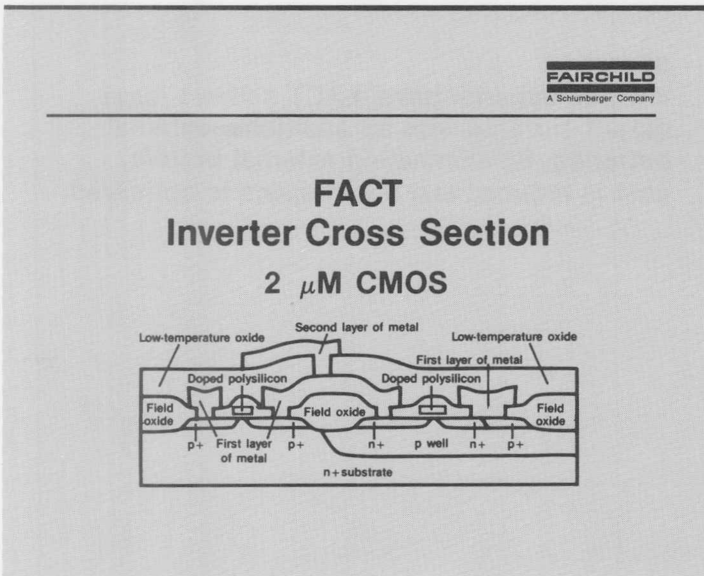
74HC/HCT Type Inverter Cross Section

3-5 μM CMOS



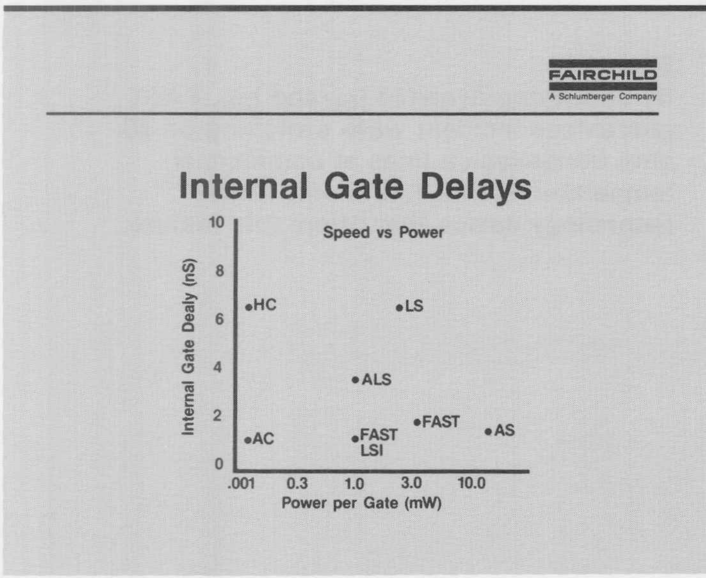
Slides 1.41, 1.42
For the 74C and 4000 series, a 5 to 6 micron metal gate process was used. A slightly improved 3 to 5 micron polysilicon gate process was used for the HC and HCT families.

Characteristics Overview



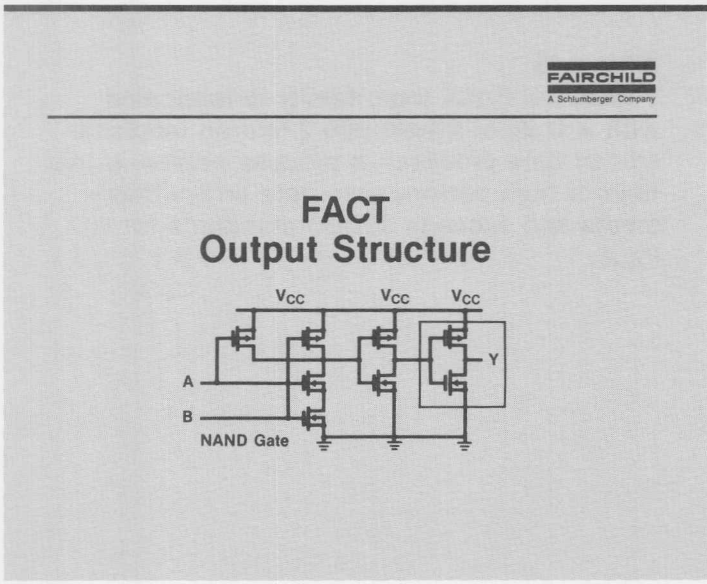
Slide 1.43
Today, the FACT logic family is fabricated with a state-of-the-art sub 2 micron isoplanar silicon gate process—a process proven in the field of high performance gate arrays that meets and exceeds JEDEC standards for HC logic.

Characteristics Overview



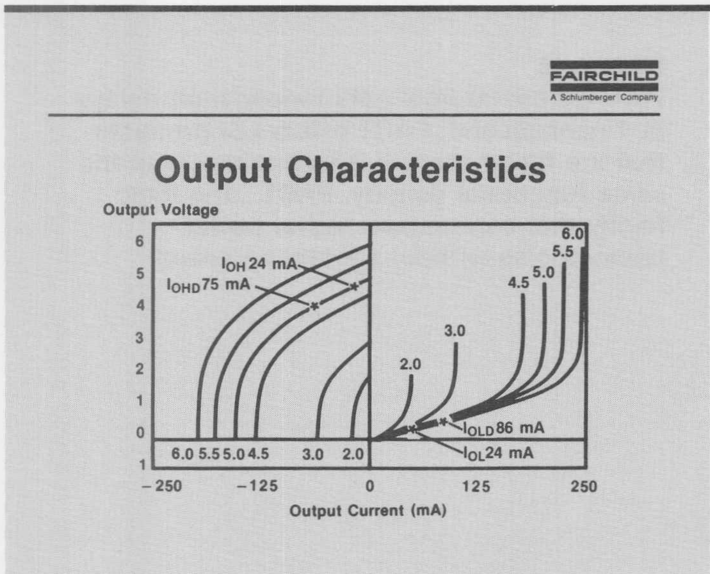
Slide 1.48
With typical internal gate propagation delays at 1 nanosecond, FACT offers LSI products that are faster than ALS technology with the same functional density. FACT....the logic family that can replace higher power technologies without sacrificing speed.

Characteristics Overview



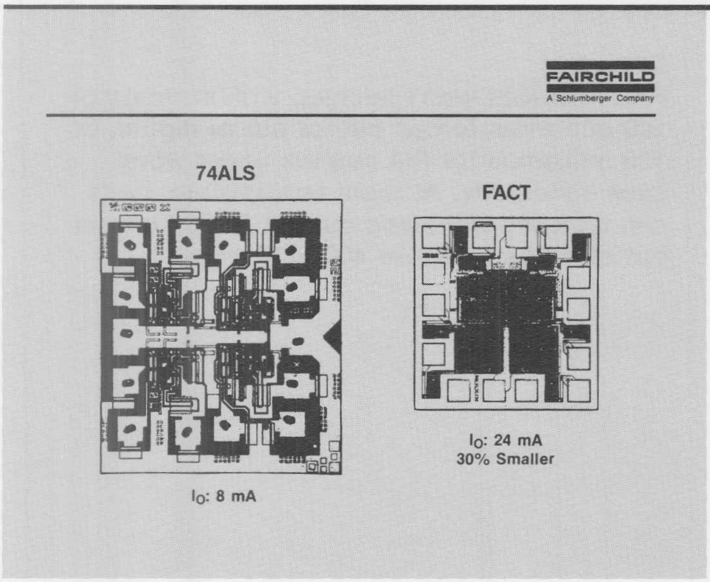
Slide 1.52
With its superior drive, FACT delivers large output currents with no additional external buffering. By eliminating external buffers, cost is reduced and board space is optimized.

Characteristics Overview



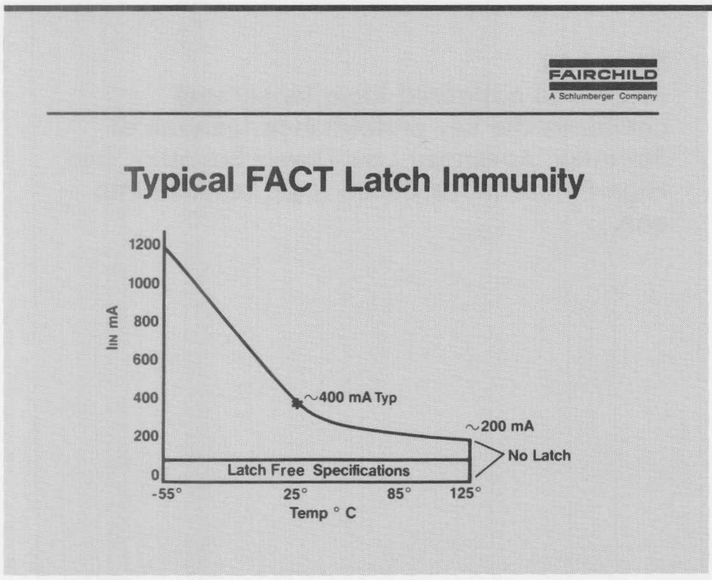
Slide 1.54
By specifying dynamic I_{OL} and I_{OH}, FACT guarantees incident wave switching on 50 ohm transmission lines at commercial temperatures. FACT...the only CMOS technology device that offers this feature.

Characteristics Overview



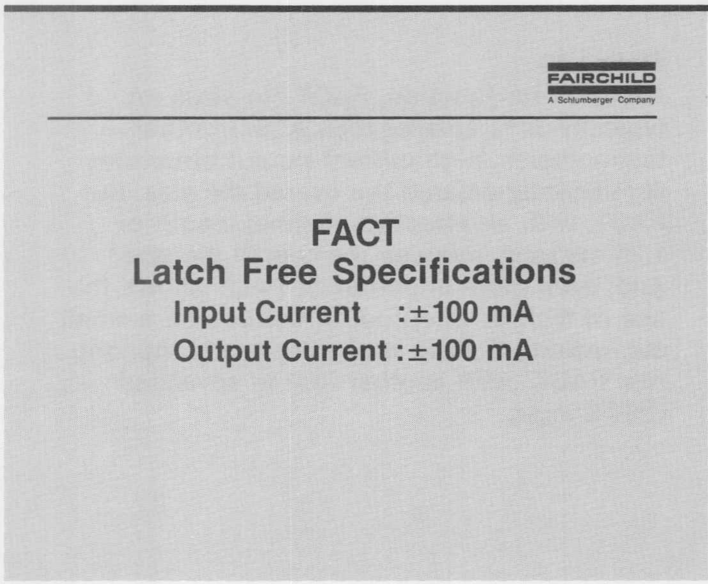
Slide 1.56
Function for function, FACT die sizes are typically 30% smaller than ALS. In other technologies, high current output structures significantly enlarge the overall die size. But FACT, with an effective channel length of 1.25 microns, reduces the overall die size. And, even more importantly, FACT allows the use of high drive output structures on a small die, making it more cost effective in the long run. FACT...with another first in advanced CMOS logic.

Characteristics Overview



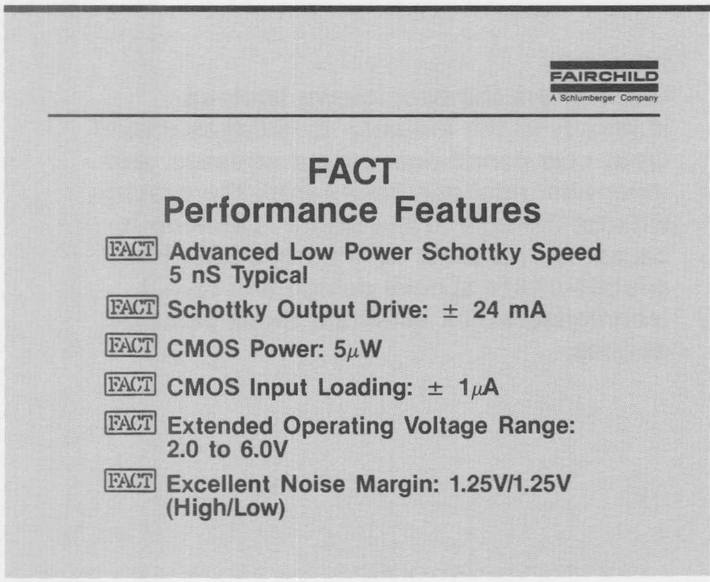
Slide 1.61
FACT offers the best known latch-up immunity in the industry. It tolerates invalid input bias conditions, output stresses, and other abnormal conditions from the system without damage to the device. Latch-up is caused by parasitic devices or SCRs. FACT circuits utilize special design and layout techniques which eliminate these parasitic devices.

Characteristics Overview

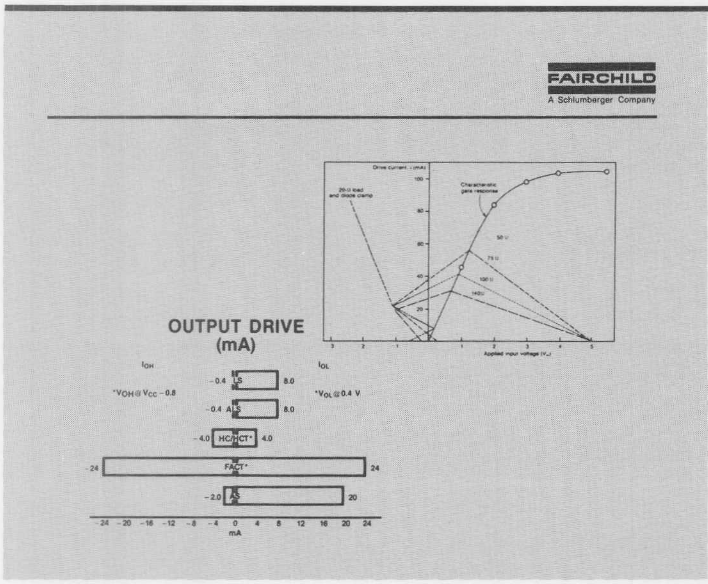


Slide 1.64
FACT devices won't latch-up with currents of 100 milliamps forced into or out of inputs, or 100 milliamps for the outputs under worst case conditions. At room temperature, parts can typically withstand current forced into or out of outputs of over 400 milliamps.

Characteristics Overview



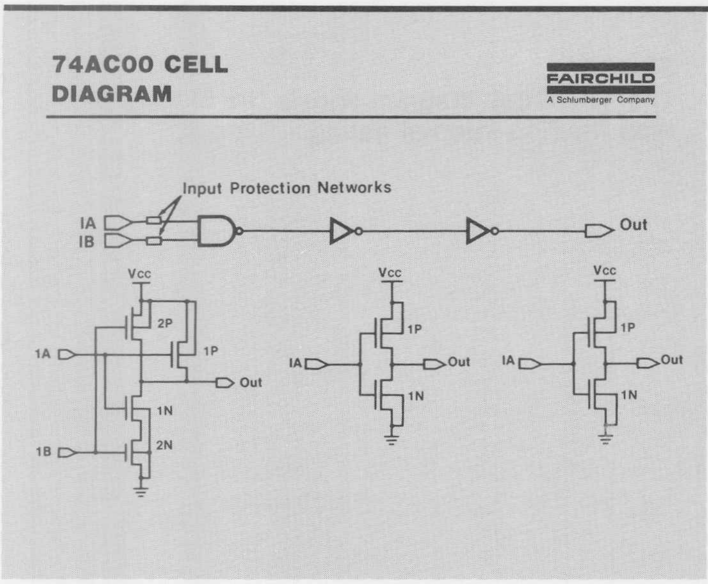
Slide 1.68
FACT—an optimized logic family that combines the key performance features of Schottky, Advanced Low Power Schottky, and High Performance CMOS logic families into one.



Slide 1.70
The result? A versatile family offering very high speed, low power consumption, superior line driving, high noise immunity, wide fanout capability, an extended power supply range and high reliability.

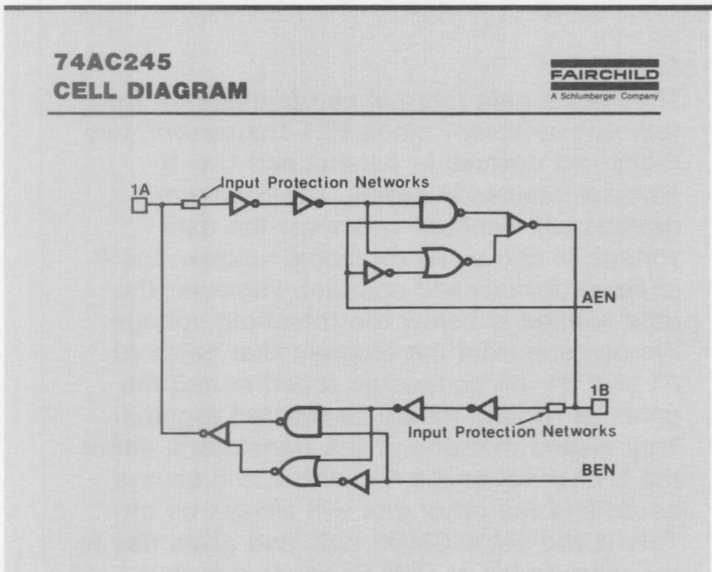
FACT—the logic family of the future.

Schematics



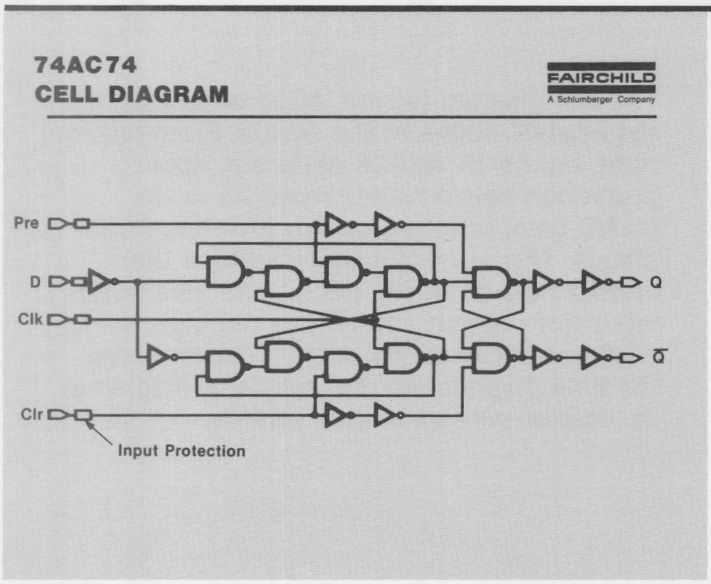
Slide 2.1
The cell diagram for the 'AC00 shows all of the internal nodes of the device. From left to right, inputs 1A and 1B enter the input protection networks and move on to the NAND gate, followed by two inverting buffer stages. This is necessary to achieve the correct polarity of the output and also buffer input from output and to give the high levels of current drive at the output. Shown below the gate diagram are the transistor diagrams associated with each gate section.

Schematics



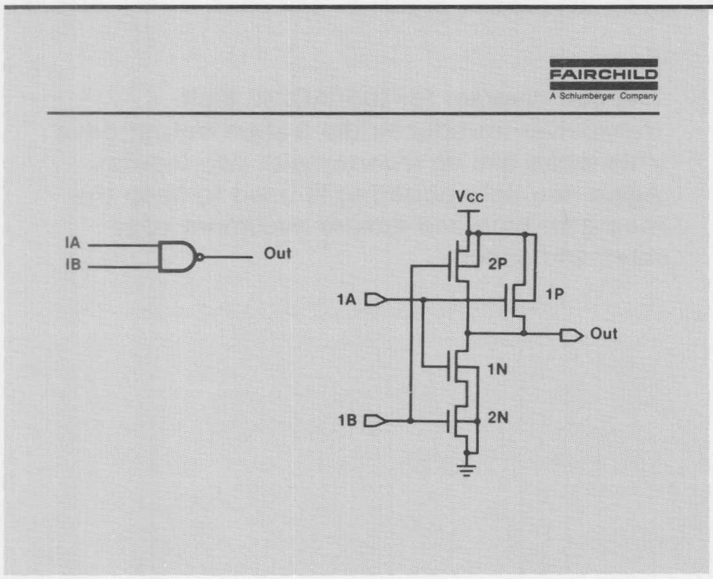
Slide 2.2
The cell diagram for the 'AC245 8-bit transceiver introduces the 3-state output drive (this looks like an inverter with two inputs). Again, multiple buffering is used to keep the loop gain high and ensure maximum edge rates and speed.

Schematics



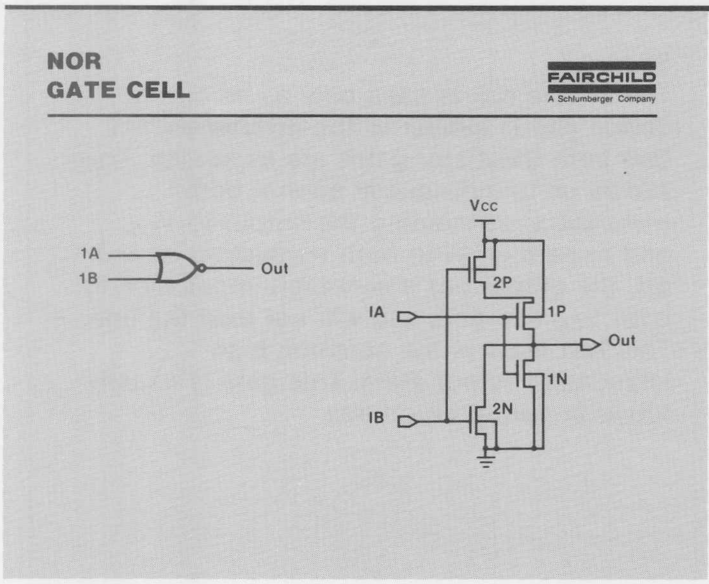
Slide 2.3
The 'AC74 cell diagram shows the classic D-type flip-flop internal gating.

Schematics



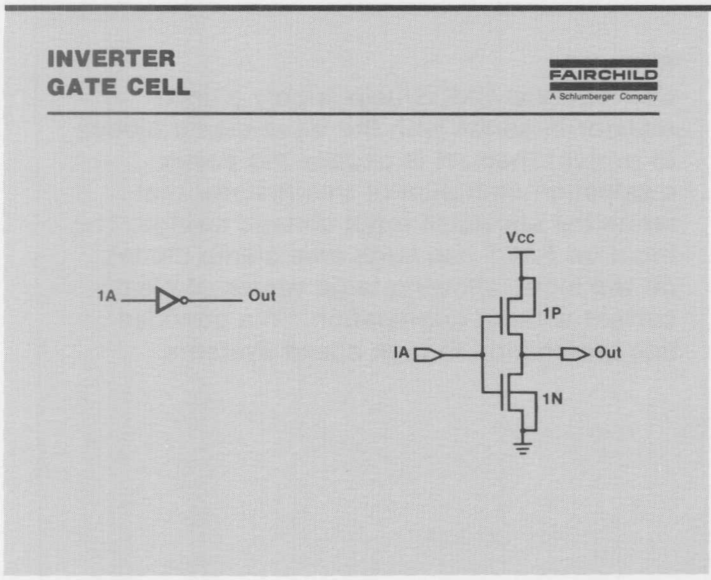
Slide 2.4
The NAND gate internal cell is made up from four enhancement mode FET transistors, two P-channel devices in parallel and two N-channel devices in series. The N-channel devices will conduct whenever the gate voltage is above the threshold voltage; the P-channel devices will conduct whenever the gate voltage is below the threshold voltage. We can see from the diagram that gates of P1 and N1 are connected together and the gates of N2 and P2 are connected together. This means that one of the transistors, either the N-channel or the P-channel, will always be on and the other one will always be off. This is the basic CMOS cell, and gives rise to the advantages of CMOS; i.e., low output impedance, balanced outputs, and low power. When both inputs A and B are high, both N-channel devices will be on, causing the output to be low. If either of the inputs are low, at least one P-channel device will be on and at least one N-channel device will be off, causing the output to be high. This is how we accomplish the NAND function.

Schematics



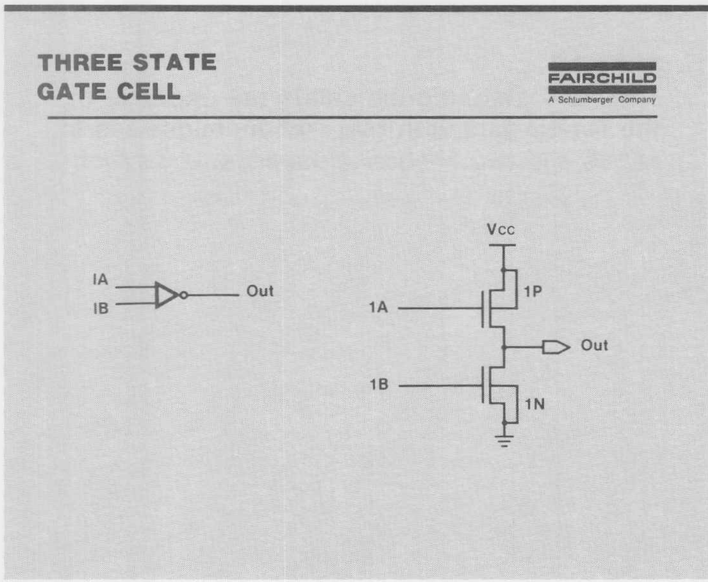
Slide 2.5
The NOR gate internal cell is the opposite of the NAND gate with two P-channel devices in series and two N-channel devices in parallel.

Schematics



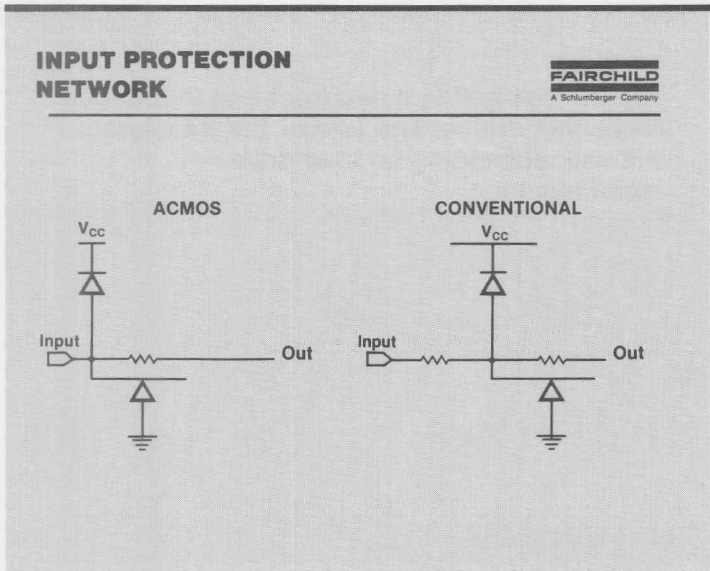
Slide 2.6
The inverter cell is made from one P- and one N-channel device. The size of the transistors will vary depending on load drive requirements.

Schematics



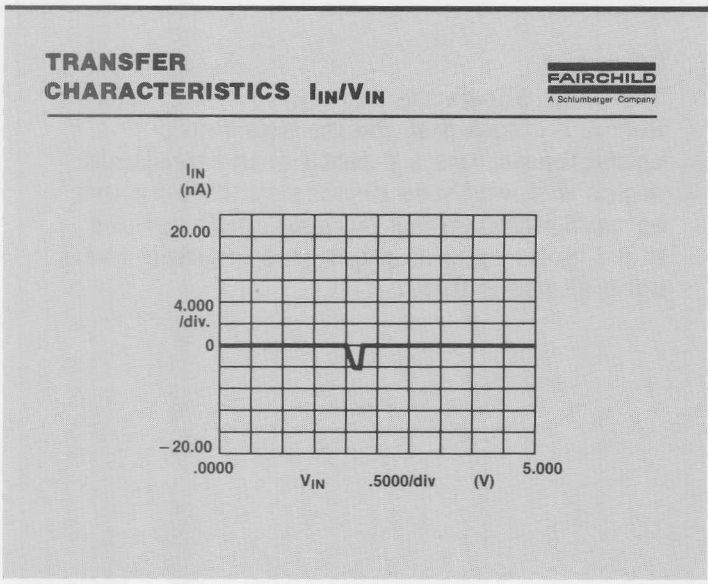
Slide 2.7
The 3-state cell is used only as an output device and is similar to the inverter except that both transistor gates are separated. This allows us to individually control both transistors, connecting the output to V_{CC}, gnd or neither. With both transistors turned off, the output has a very high impedance to both V_{CC} and gnd, and will not load the line. This last state is the common high-impedance output state. This gate is usually found in output structures.

Input Characteristics



Slide 2.8
Conventional CMOS uses a poly silicon resistor in series with the input clamp diodes to protect them. It is usually the power dissipation limitation of this resistor that limits the allowable input voltage swings. The input on FACT has large area clamp diodes on the input, allowing large values of clamp current without degradation. This provides line termination in high speed systems.

Input Characteristics



Slide 2.9
The input transfer characteristic shows almost zero input current requirements. The small excursion at the input threshold is caused by the change in input Miller capacitance as the input switches and is normal for all CMOS devices.

Input Characteristics

INPUT SPECIFICATIONS

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−40°C Thru 85°C Guaranteed Values

Parameter		AC	ACT	V_{CC}
V_{IH}	Input High Voltage	2.0V 3.15V 3.85V	2.0V 2.0V	3.0V 4.5V 5.5V
V_{IL}	Input Low Voltage	0.9V 1.35V 1.65V	0.8V 0.8V	3.0V 4.5V 5.5V
I_{IN}	Input Current	± 1.0μA	± 1.0μA	5.5V
C_{IN}	Input Capacitance	<5 pf	<5 pf	3.0-5.5V

Slide 2.10
As we have shown previously, FACT specifies guaranteed input parameters over the −40 degree to +85 degree C temperature range for AC and ACT (TTL input levels). Three voltages specifications are given for AC, 3.0V, 4.5V, and 5.5V, while ACT is specified at two voltages, 4.5V and 5.5V.

Output Characteristics

TRANSFER CHARACTERISTICS V_{IN}/V_{OUT}

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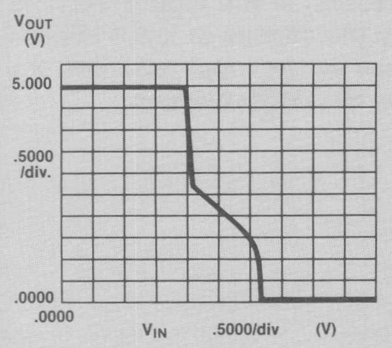

Slide 2.11
This slide shows the V_{IN} V_{OUT} transfer curve for FACT. Note that the transfer characteristic has a plateau at the threshold region making these devices suitable for use as oscillators, unlike 74C and 74HC devices that require special unbuffered inverters to be used as oscillators.

Output Characteristics

OUTPUT SPECIFICATIONS

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– 40 °C Thru 85 °C Guaranteed Values

	Parameter	Condition	AC	ACT	V_{CC}
V_{OH}	Output Voltage High	$I_{OH} = -20\mu A$	2.9V 4.4V 5.4V	 4.4V 5.4V	3.0V 4.5V 5.5V
		$I_{OH} =$ – 4mA – 24mA – 24mA	2.46V 3.76V 4.76V	 3.76 4.76	3.0V 4.5V 5.5V
V_{OL}	Output Voltage Low	$I_{OL} = 20\mu A$	0.1V 0.1V 0.1V	 0.1V 0.1V	3.0V 4.5V 5.5V
		$I_{OL} =$ 4mA 24mA 24mA	0.37V 0.37V 0.37V	 0.37V 0.37V	3.0V 4.5V 5.5V
I_{OH}	Output Current High	$V_O = 3.85V$	– 75mA	– 75mA	5.5V
I_{OL}	Output Current Low	$V_O = 1.1V$	86mA	86mA	5.5V
I_{OZ}	Output Leakage Current 3 State	$V_O = V_{CC}$ or Gnd	± 5μA	± 5μA	5.5V
C_O	Output Capacitance	3 State	10 pf	10 pf	3.0-5.5V

Slide 2.12
These are the guaranteed output parameters over the – 40 to + 85 degree C temperature range for AC and ACT devices. As with the input ratings, AC is specified for three voltages and ACT is specified for two.

Output Characteristics

ESD
TEST CIRCUIT

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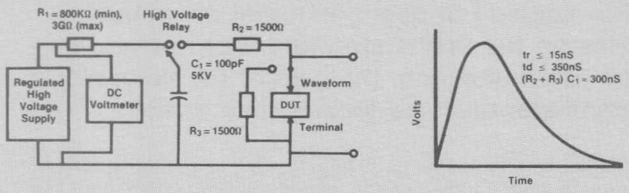

Slide 2.13
FACT shows excellent resistance to ESD type damage. Devices are tested to Mil Std 883C, TP-3015, during characterization and yield better than 3KV.

Output Characteristics

ESD NODE
TABLE

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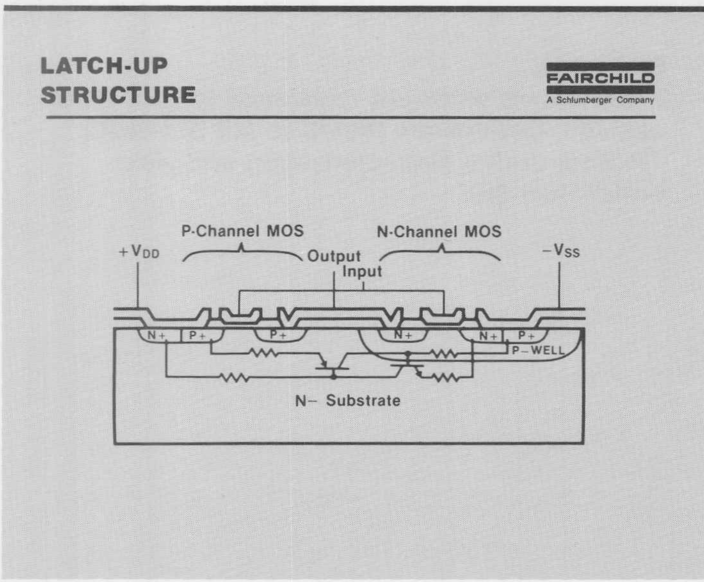
Functional Application

- Input to Common
- Output to Common
- Supply Voltage(s) to Common
- Input to Supply
- Output to Supply

Slide 2.14
All nodes are tested to each other as shown in the table.

Output Characteristics



Slide 2.15
A major problem with CMOS has been its sensitivity to latch-up, due usually to high parasitic gains and high input impedance. Shown here is the parasitic PNPN structure. For latch-up to occur, external drive must bias on the PNPN structure. For latch-up to be self-sustaining, the gain of the parasitic transistor must be greater than one.

Output Characteristics

ANTI LATCH-UP ENHANCEMENTS

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- Process Ensures Beta of Parasitic PNPN Structure <1
- Low Substrate and P well Resistivity
- IC Design and Layout
- Sustained Latch Up Eliminated

Slide 2.16
FACT devices have been specifically designed to reduce the possibility of latch-up occurring and also that any latch-up cannot be self-sustaining. The Fairchild FACT process ensures that the parasitic transistors have sufficiently low betas so that self-sustaining latch-up cannot occur. Low substrate and P-well resistivity increase external drive current required to cause a parasitic to turn on. Careful design layout minimizes the substrate-injected current coupling to other circuit areas.

Output Characteristics

LATCH-UP PREVENTION

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- Ensure V_{CC} Never Exceeds 7V
- Current Limit Inputs with 100Ω Resistor
- Diode Clamp Inductive Loads ie Relays
- Terminate Long Transmission Lines
- Maintain Environment within Temperature Specification

Slide 2.17
Latch-up can be avoided by staying within the data sheet limits and minimizing any current injection into or out of the device inputs and outputs.

Military Specifications

AEROSPACE & DEFENSE SPECIFICATION PROGRAM

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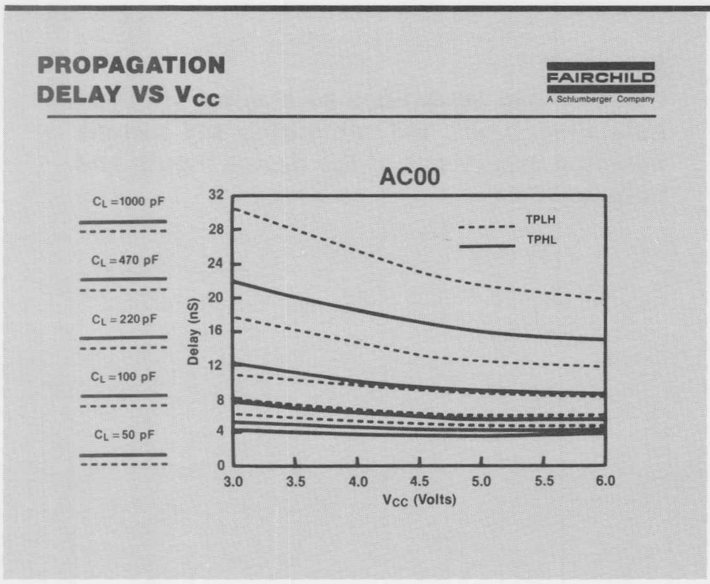
- Introduce Devices Tested Over Military Temperature Ranges
  −55°C to 125°C
  Concurrent with Commercial Introduction
  Ceramic Dual-in-Line Package (DM)
- Compliant to Military Standard 883 Revision C
  To Follow Initial Introduction by Two Months
  Approval in all Three Military Packages
- Certification to DESC Drawing Program
  Starting Mid 1986 on Current Devices
  Subsequent Devices to Follow One Month After
  MIL-STD 883 Approval

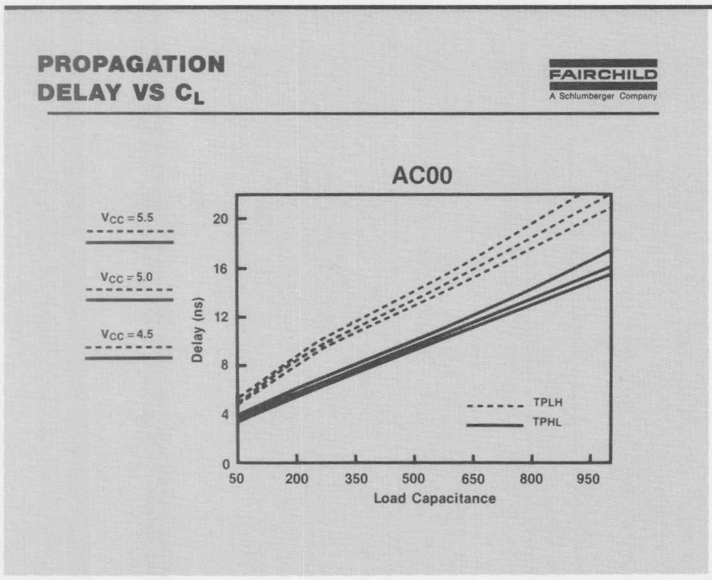
Slide 2.18
Notes.

AC Performance



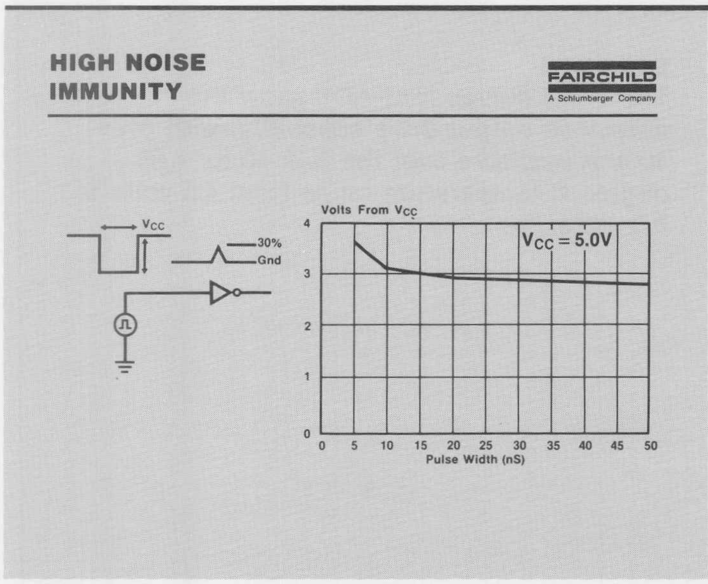
Slide 2.19
FACT shows very little change in propagation delay over the 3 to 6 volt V_{CC} range, even with very large capacitive loads.

AC Performance



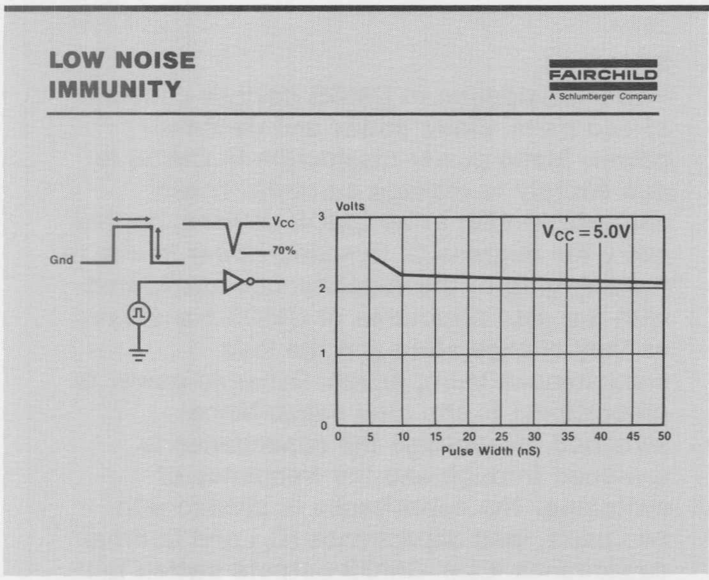
Slide 2.20
Changes to effective propagation delay with load capacitance are minimized with the high output drive capabilities of FACT. FACT has a derating factor of 13 to 19 ps/pf, while ALS devices are derated at 32 ps/pf and HC devices are derated at 250 ps/pf.

AC Performance



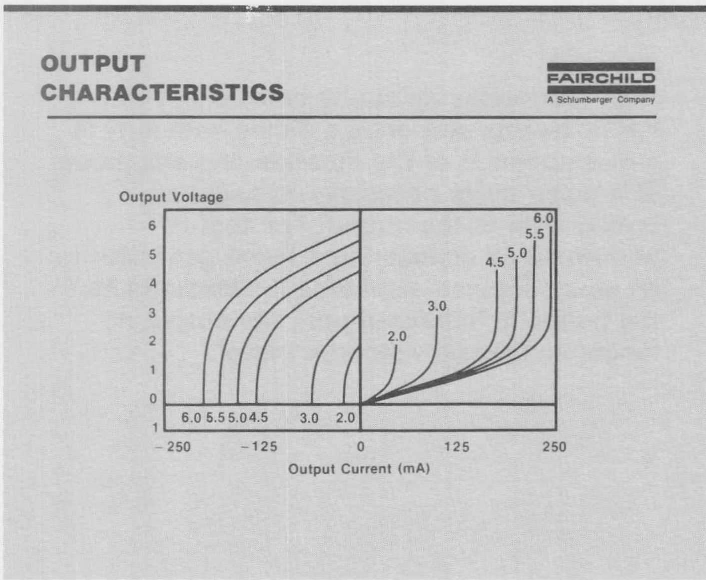
Slide 2.21
High level noise immunity is excellent with FACT, as this plot shows. Noise immunity is a measurement of the duration and amplitude of a noise pulse necessary to cause an invalid level at the output. The test is performed by connecting a pulse generator to an input. A pulse amplitude is selected and the period is increased until the output no longer sustains a valid input level.

AC Performance



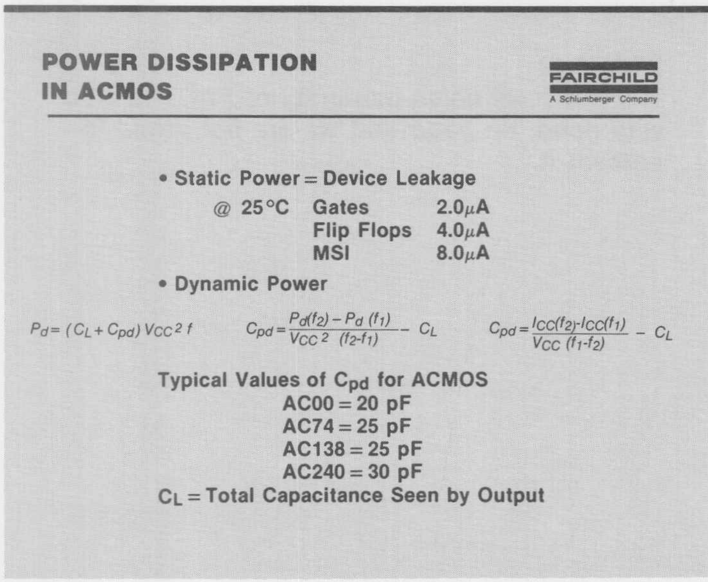
Slide 2.22
The low level noise immunity of FACT is also very good. So good that we are not afraid to present it.

AC Performance

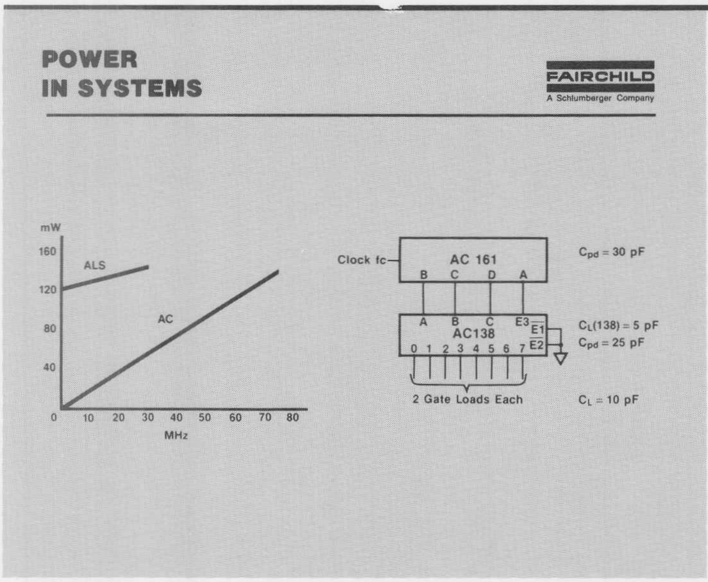


Slide 2.23
The V_O/I_O curves for FACT show the enhanced output drive capability, with over 100mA available over the full -40 to +85 degree C temperature range from 4.5 volts to 5.5 volts.

Power Dissipation

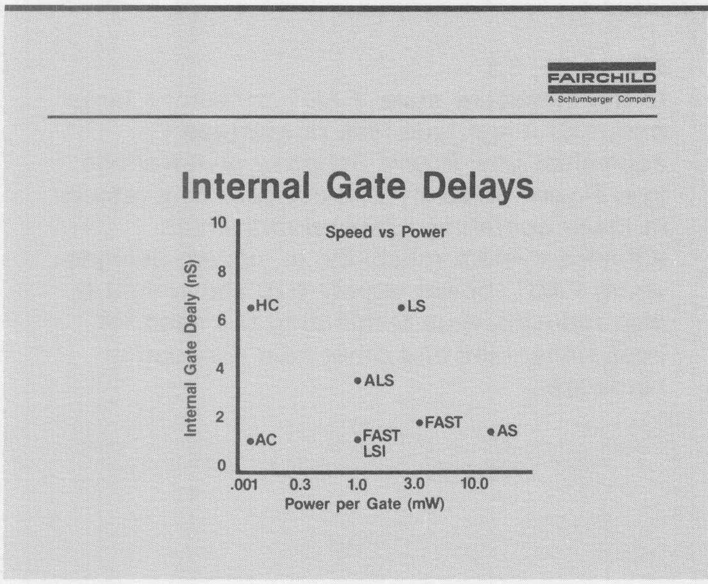


Slide 2.24
Power dissipation in CMOS devices consists of two parts, static power and dynamic power. Static power dissipation in CMOS is due entirely to leakage currents. These currents, similar in all CMOS devices, double every ten degrees C. Dynamic power is due to the charging of the capacitances associated with the gate structures of CMOS transistors as they change state and the load capacitances being driven. Dynamic power is proportional to the total capacitance switched, the voltage the capacitance is switched through and the frequency of switching. The capacitance is divided into two parts, load capacitance (C_L) and internal capacitance (C_{pd}). CMOS outputs switch rail to rail, unlike bipolar devices which switch typically 0.4 to 3.0 volts—approximately 2.6 volts, almost half that of CMOS on the same power rails. This large swing is responsible for CMOS's extended noise margins.

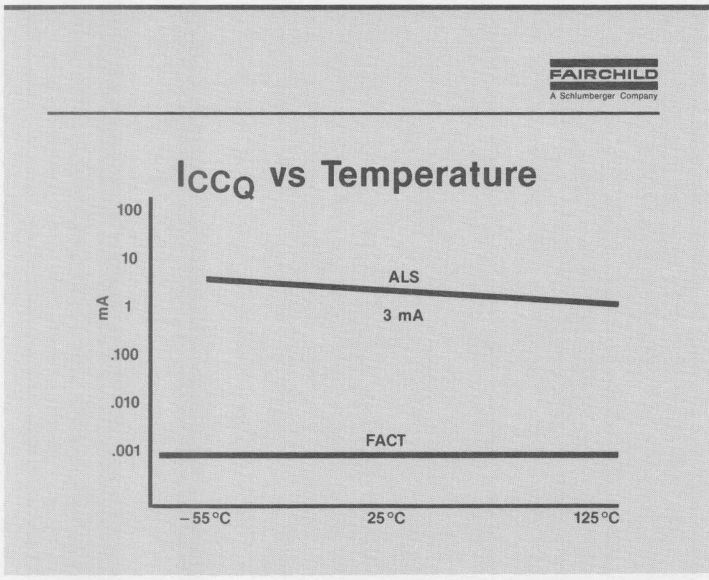


Slide 2.25

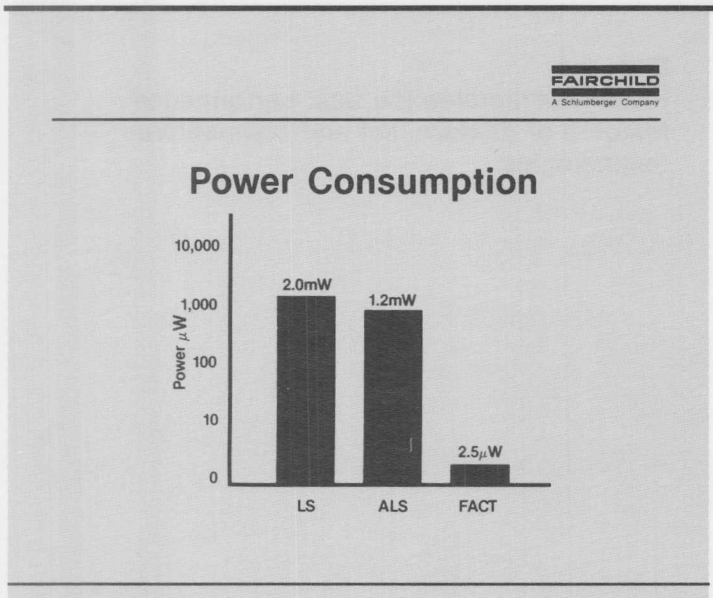
To determine power in a system, we must evaluate each frequency component and total the power at all frequencies. Here we show a very simple system, a '161 binary counter driving a '138 decoder. This generates eight non-overlapping clock phases. First, we will evaluate the '161. Its static power dissipation is due purely to static I_{CC} currents and is $I_{CCS} \bullet V_{CC}$. Its internal nodes will be switching at F_C, so the dynamic power dissipated within the chip is $F_C \bullet C_{pd(161)} \bullet V_{CC}^2$. The '161 is also driving four loads, with each load switching at a divided value of F_C. Each node will dissipate both static and dynamic power. The static power is related to the leakage current and can be calculated by the formula $I_L \bullet V_{CC}$. The dynamic power dissipated is related to its switching frequency, F_S, the capacitive value of the load, C_L, and the voltage swing the load sees, V_S. The formula for this is $F_S \bullet C_L \bullet V_S^2$. Output A of the '161 is switching at $F_C/2$, B switches at $F_C/4$, C switches at $F_C/8$, and D switches at $F_C/16$. The total power dissipated by the loads is the sum of these or $(15/16\ F_C) \bullet C_L \bullet V_S^2$. We do the same calculations for the '138. Of course there is the static power, which is calculated the same as for the '161. The dynamic power is almost identical to the '161, except that the frequency is divided by 2, because this is the maximum frequency into the '138. Therefore, the dynamic power dissipation in the '138 is $\frac{1}{2} \bullet F_C \bullet C_{pd(138)} \bullet V_{CC}^2$. Again, we also have to calculate the static and dynamic load power. Each of the sixteen '138 loads (2 per output) will dissipate power. Remember that only two will be low at any one time. This is important when calculating power for technologies that have unbalanced input leakage currents, e.g., ALS. Each load will switch at a frequency of $F_C/16$, so that the total dynamic load power will be equal to $16 \bullet (F_C/16) \bullet C_L \bullet V_S^2$. The total system power is a combination of all of this power. This graph compares the power dissipated by this circuit built in FACT and ALS vs frequency.

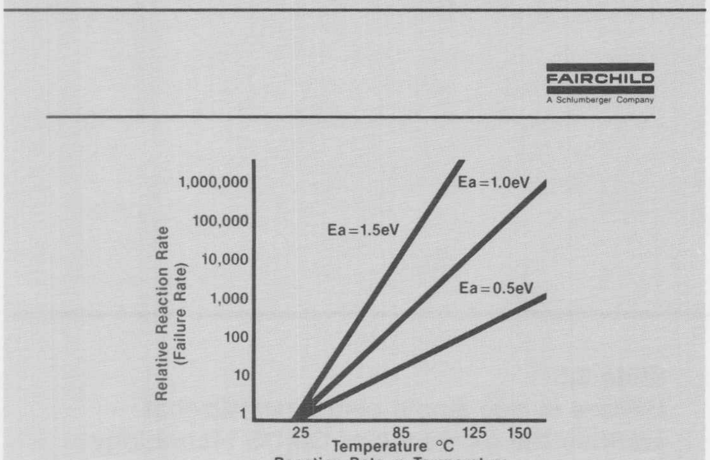


Slide 3.4
FACT incorporates the best performance features of predecessor and competitive technologies.



Slide 3.5
If there is one single characteristic that justifies the existence of CMOS technology logic, it's ultra low power consumption. FACT...the device that offers this low power feature without sacrificing speed.





Reaction Rate vs Temperature
(Normalized to +25°C)

Slides 3.7, 3.8

In the quiescent state, FACT consumes three orders of magnitude less power than equivalent Low Power Schottky or Advanced Low Power Schottky TTL devices. This results in lower operating temperatures which enhance system reliability. In system designs using FACT, power supply size and weight is also reduced, thus eliminating the need for heat sinks, fans and other heat dissipation hardware.

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LS	400 μA/Gate
ALS	200 μA/Gate
FACT	0.5 μA/Gate
HC/HCT	0.5 μA/Gate

Slide 3.10
When compared to LS and ALS technologies, FACT has an extremely low quiescent current drain which is equivalent to that of HC or high performance CMOS logic.

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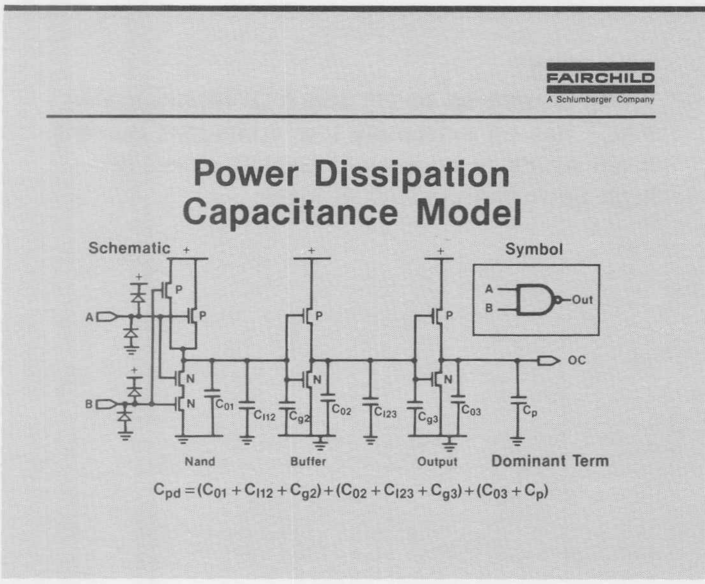
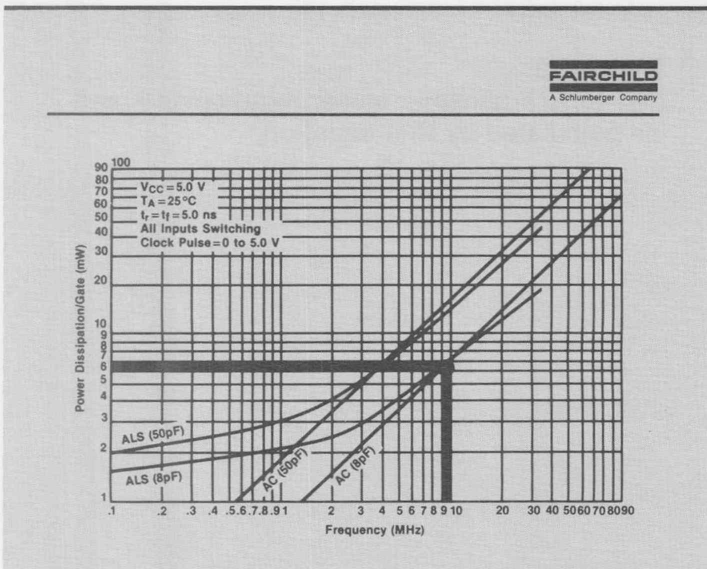
$$Pd = (C_L + C_{pd}) + V_{CC}^2 \times F$$

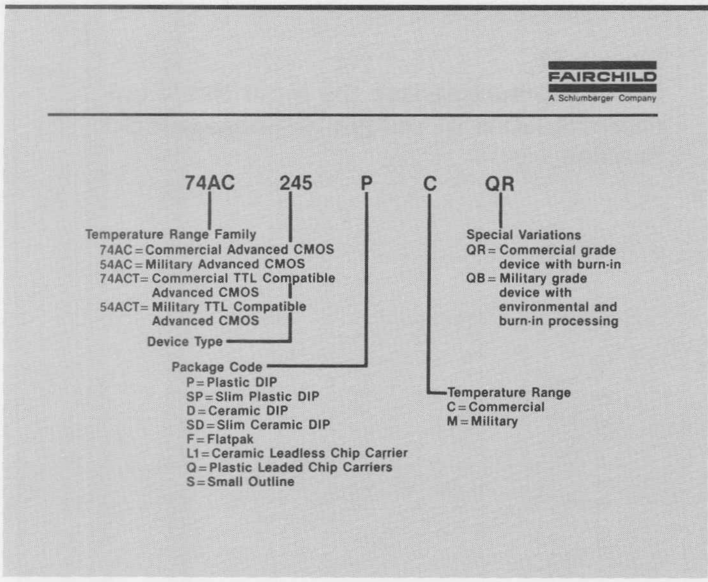
Slide 3.13
The device dynamic power requirements can be calculated by this equation.



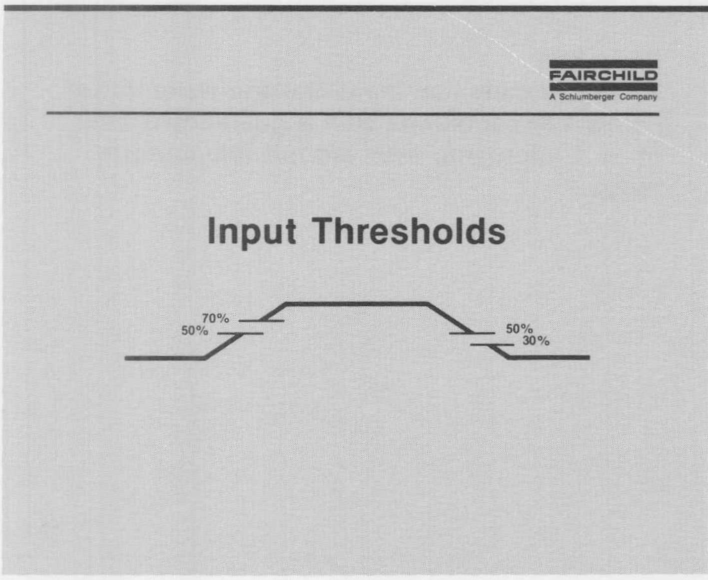
Slide 3.14
Here, F is the frequency in Hertz; C_L is the total load capacitance present at the output under test in picofarads. C_{pd} is a measure of internal capacitance given specifically for power consumption calculations. C_{pd} is typically 25 picofarads for a logic gate function.



Slide 3.17
This graph compares FACT's dynamic power consumption to ALS with two load capacitances—8 and 50 picofarad.



Slide 3.20
To optimize interfacing with various technology logic families, FACT has been designed with two types of input thresholds, CMOS and TTL. Devices with CMOS input threshold levels are designated by 74ACXX while the TTL compatible input devices are designated by 74ACTXX.



Slide 3.22
With the 74AC devices, the input thresholds are based on a percentage of the V_{CC} value. That is, $V_{IH} = 70\%$ of V_{CC} and $V_{IL} = 30\%$ of V_{CC}.

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V_{IH}/V_{IL}

	74ALS	74HC	74HCT	74AC	74ACT	Units
(Min)	2.0	3.15	2.0	3.15	2.0	Volts
(Max)	0.8	0.9	0.8	1.35	0.8	

Slide 3.23
This table summarizes the input threshold characteristics of various technology logic families.

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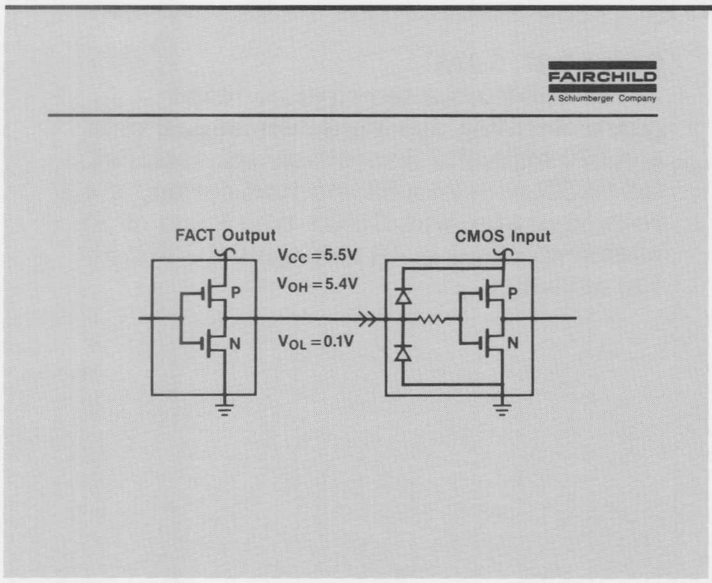
Typical Input Leakage Below 100 nA Guaranteed ± 1 μA at All Operating Temperature Ranges

Slide 3.25
FACT typically has input leakage currents far below 100 nanoamps with a guaranteed limit of ± 1 microamp over the full temperature range.



Slide 3.26
Both 54 and 74AC, and 54 and 74ACT devices have CMOS output stages that can transition within 100 millivolts from either power supply rail when driving CMOS type loads at 20 microamps. FACT outputs perform very well under heavier load conditions as well.

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DC Characteristics for AC Family Devices.

Symbol	Parameter	Conditions	V_{CC}	54AC/74AC $T_A = 25°$		54 AC $T_A = -55°$ to $+125°C$	74AC $T_A = -40°$ to $+85°C$	Units
				Typ	Guaranteed Maximum			
V_{OH}	Minimum High Level Output Voltage	$V_{IN} = V_{IL}$ or V_{IH} $I_{OUT} = -20\ \mu A$	3.0 4.5 5.5	2.99 4.49 5.49	2.9 4.4 5.4	2.9 4.4 5.4	2.9 4.4 5.4	V
		I_{OH} −4 mA −24 mA −24 mA	3.0 4.5 5.5		2.56 3.86 4.86	2.4 3.7 4.7	2.46 3.76 4.76	V
V_{OL}	Maximum Low Level Output Voltage	$V_{IN} = V_{IL}$ or V_{IH} $I_{OUT} = 20\ \mu A$	3.0 4.5 5.5	.002 .001 .001	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		I_{OL} 4 mA 24 mA 24 mA	3.0 4.5 5.5		0.32 0.32 0.32	0.4 0.4 0.4	0.37 0.37 0.37	

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DC Characteristics for ACT Family Devices.

Symbol	Parameter	Conditions	V_{CC}	54ACT/74ACT $T_A = 25°$		54 ACT $T_A = -55°$ to $+125°C$	74ACT $T_A = -40°$ to $+85°C$	Units
				Typ	Guaranteed Maximum			
V_{OH}	Minimum High Level Output Voltage	$V_{IN} = V_{IL}$ or V_{IH} $I_{OUT} = -20\ \mu A$	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	4.4 5.4	V
		I_{OH} −24 mA −24 mA	4.5 5.5		3.86 4.86	3.7 4.7	3.76 4.76	V
V_{OL}	Minimum Low Level Output Voltage	$V_I = V_{IL}$ or V_{IH} $I_{OUT} = 20\ \mu A$	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	0.1 0.1	V
		I_{OL} 24 mA 24 mA	4.5 5.5		0.32 0.32	0.4 0.4	0.37 0.37	V

Slides 3.27, 3.27A

At the commercial temperature range, guaranteed V_{OH} and V_{OL} levels of 3.76 volts and 370 millivolts respectively are specified for FACT, with 24 milliamp load current at 4.5 volts V_{CC}. And, with CMOS type loads of 20 microamps, V_{OH} is 4.4 volts and V_{OL} equals 100 millivolts.

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DC Noise Margin Low/High

74LS	74LS	74HC	74AC	Units
0.3/0.7	0.4/0.7	0.8/1.25	1.25/1.25	Volts

Slide 3.28
Knowing these figures and the input thresholds for FACT, we can compare its DC noise margin characteristics with other technology logic families. This table shows the noise margin in volts for LS, ALS, HC and FACT or AC logic families.

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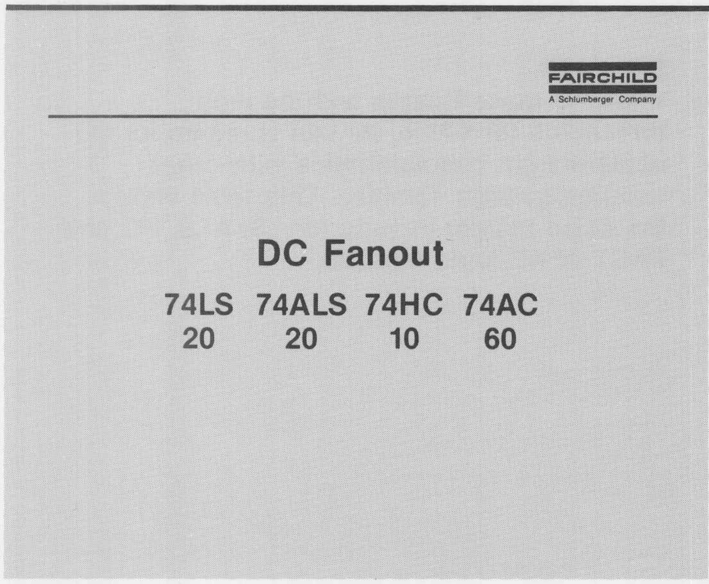
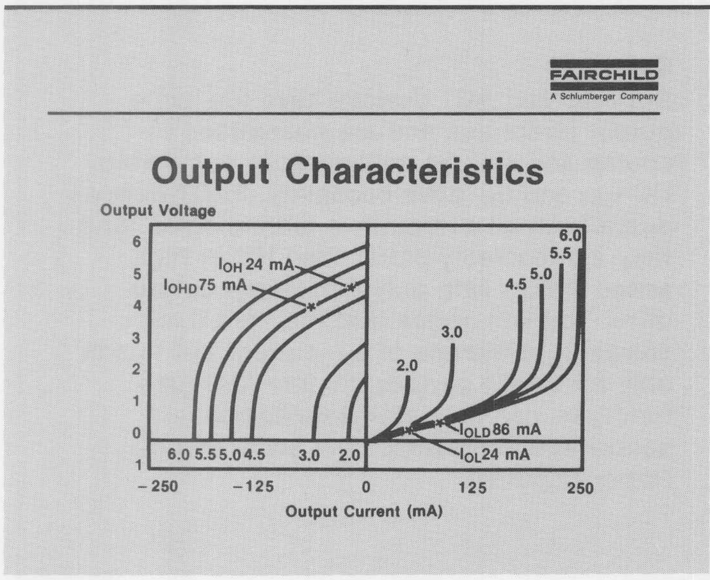
I_{OL}/I_{OH} Characteristics

74AC:	24/−24 mA
74ALS	24/−15 mA
74LS	8/−0.4 mA
74HC	4/−4 mA

Slide 3.29
Both AC and ACT devices have the same output structures and are guaranteed to source and sink 24 milliamps. In comparing DC I_{OH} and I_{OL} drive capability, FACT devices outperform all competitive technologies. And they are markedly better than HC or high speed CMOS with only 4 milliamp output drive. You will notice that the 74ALS logic shows 24 milliamps of I_{OL} current but this is only for select devices. Simple ALS gate functions can only sink 8 milliamps and source 400 microamps...the same as Low Power Schottky!



Slide 3.32
FACT's high output drive also allows wide fanout. With 24 milliamps of drive current, 60 Low Power Schottky inputs can be driven without external buffering.



Slide 3.34
In addition to FACT's superior DC output drive, Fairchild also specifies dynamic output drive parameters. FACT can drive 50 ohm impedence transmission lines and switch a logic device at the receiver end on the incident wave. FACT achieves this by specifying a dynamic output source current of 75 milliamps and an 86 milliamp dynamic sink current at the commercial temperature range.

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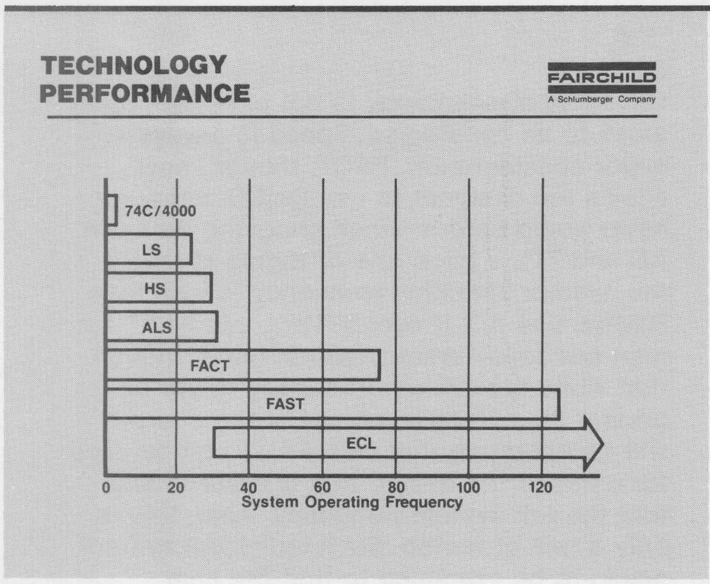
Propagation Delay (Commercial Temperature Range)

Parameter	Product No.		LS	ALS	HCMOS	FACT	Unit
Propagation Delay	74XX00	Max	15.0	11.0	23.0	9.5	nS
Clock to Output Delay	74XX74	Max	40.0	18.0	44.0	11.0	nS
Clock to Output Delay	74XX163	Max	27.0	17.0	52.0	17.0	nS
Clock Frequency		typical fmax	33	50	50	125	MHz

Conditions: (LS) $V_{CC} = 5.0$ V ± 5%, $C_L = 15$ pF, 25 °C;
(ALS/HC/FACT) $V_{CC} = 5.0$ V ± 10%, $C_L = 50$ pF,
Typ values at 25 °C, Max values at 0 °C to 70 °C. for
ALS, −40 to +85 °C for HC/FACT.

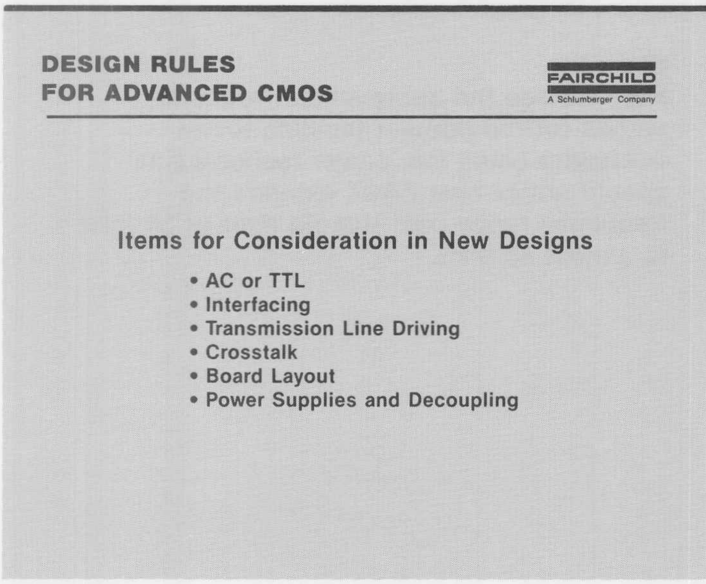
Slide 3.41

This table compares the guaranteed maximum propagation and clock edge to output delays of a quad NAND gate, a dual D-type flip-flop and a 4-bit BCD counter.



Slide 4.1
Here we see the approximate frequency ranges for the popular families today. Designers using low power technologies should notice that FACT extends the frequency range past the old limit of 30 MHz to almost 80 MHz.

Design Rules



Slide 4.2

Choosing a technology is not easy with many areas to be considered. Speed is always a major consideration. FACT, though, now allows the designer to use CMOS where he never could before. When choosing between AC and TTL a good rule of thumb is that if the system operating frequency is less than 50MHz, use AC. If over 50MHz, use FAST for high frequency areas. Keep in mind, though, that while the system frequency might be greater than 50 MHz, not all of the circuits will be operating that fast. FACT can be used for areas of the design that operate at less that the full system frequency. Also, this is only a rule of thumb. Each individual system needs to be examined to find the best technological fit.

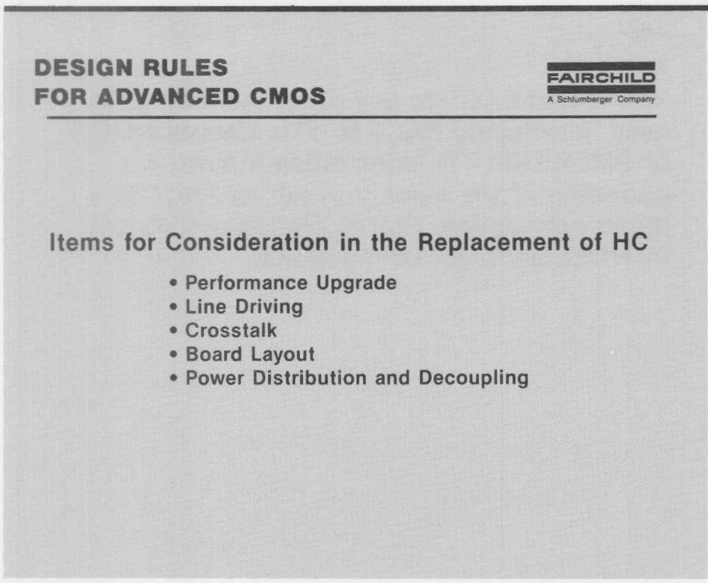
Interfacing—Inter board and technology interfaces, battery back-up and power down or live insert extract systems require some special thought.

Transmission Line Driving—AC has superior line driving capabilities to all CMOS families and most TTL families.

Crosstalk—As edge rates increase, the liability of crosstalk problems increase. The enhanced noise immunity and high threshold levels improve FACT's resistance to crosstalk problems.

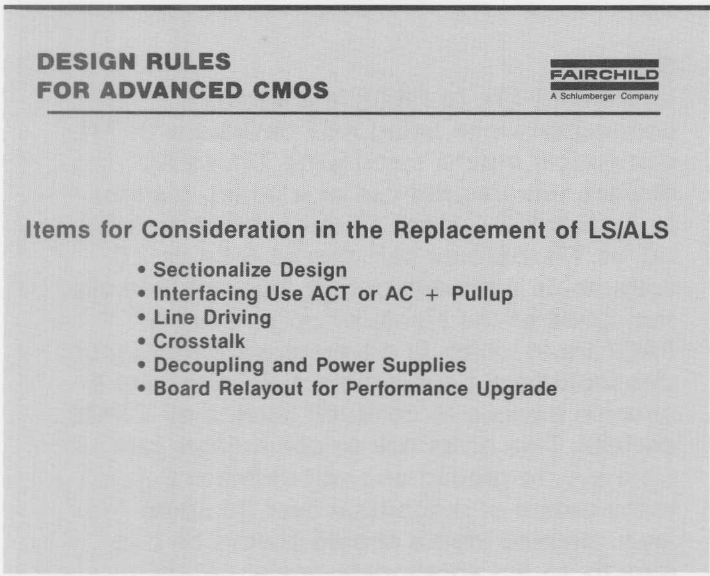
Board layout—Good board layout will ensure that a good design is trouble-free in production.

Power supplies and decoupling—Maximize ground and V_{CC} traces to keep V_{CC}/Gnd impedance as low as possible; full Gnd/V_{CC} planes are best. Decouple any device driving a transmission line, and add one capacitor for every three packages otherwise.



Slide 4.3

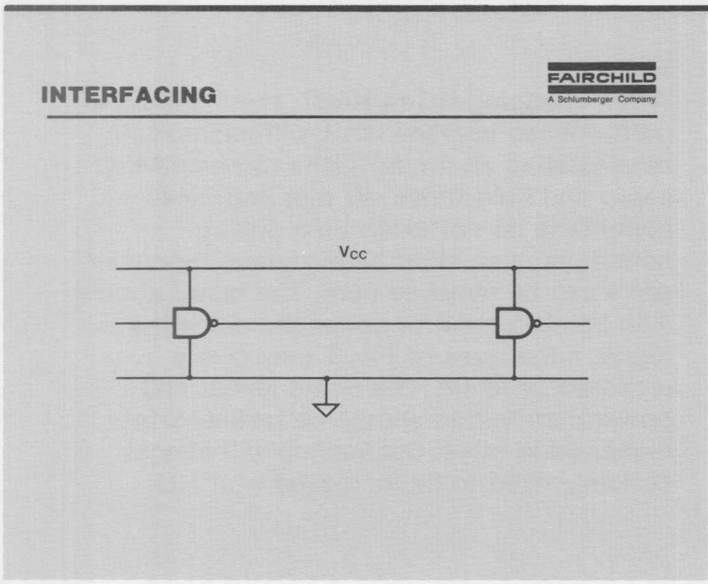
When changing HC to FACT, there will be a performance upgrade. This will necessitate recalculating all timing paths to ensure that setup and hold times are met and race conditions do not exist. Line driving conditions also must be examined. Some HC parts can be removed here. The board should also be evaluated for crosstalk, since the higher edge rates of FACT may give a crosstalk problem. The board layout and power distribution should be reviewed for higher edge rates. Decoupling will almost certainly need to be increased over HC.



Slide 4.4

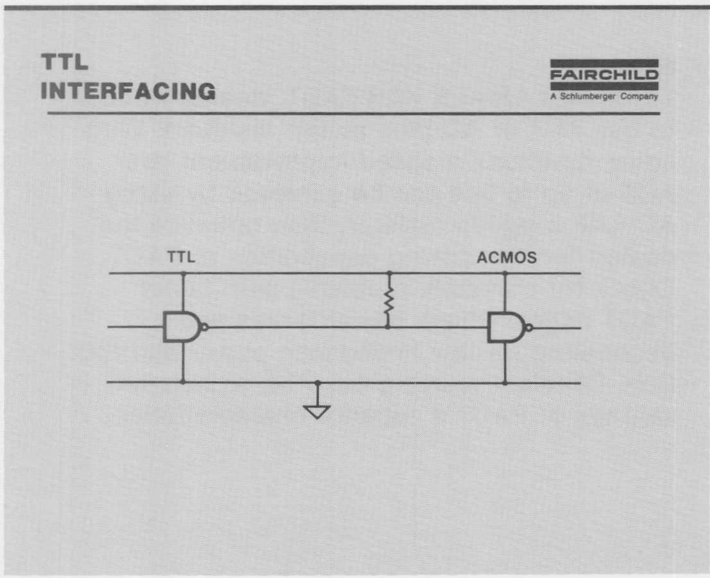
To replace LS/ALS with FACT, decide whether to use ACT or AC plus pullup resistors. With some functions a speed improvement over ACT of up to 2ns can be achieved by using AC with a pullup resistor, then optimize the design for line driving capabilities of FACT. Check for crosstalk problems with faster FACT edges. Check power traces and decoupling for low impedance power distribution. Consider relaying out PCB to take advantage of FACT's superior characteristics.

Interfacing



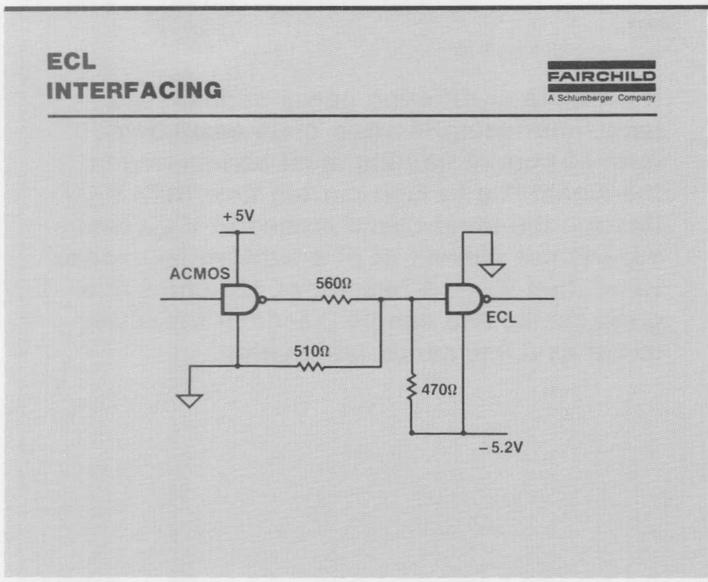
Slide 4.5
Interfacing FACT to any other technology is easy. Interfacing FACT to TTL, CMOS, NMOS or PMOS with TTL compatible inputs operating at the same V_{CC} rail as FACT is a direct connection. CMOS, NMOS and PMOS interface as direct connections.

Interfacing



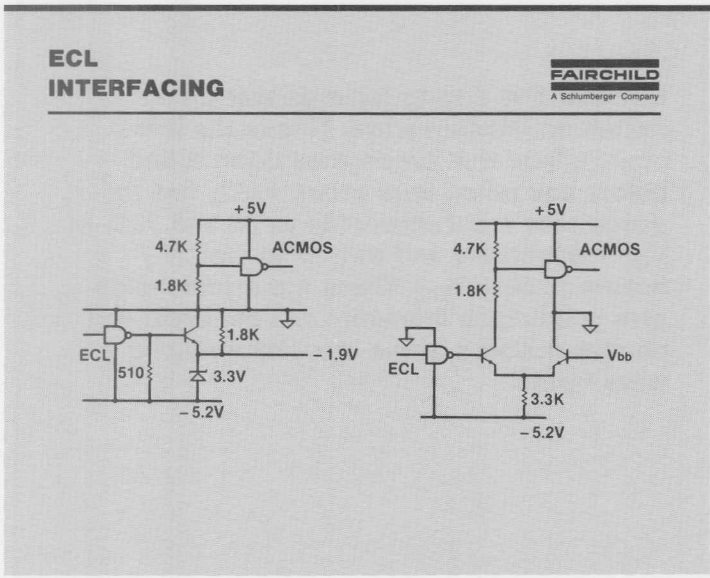
Slide 4.6
Interfacing TTL to FACT is a direct connection when using ACT devices with TTL compatible inputs. Interfacing TTL to AC devices requires the use of a pullup resistor to establish V_{IH} close to the positive supply rail as TTL outputs can give as little as 3.0 volts on an unloaded output, but can increase the speed of the signal by up to 2 ns. A FACT input which is driven close to the input threshold level causes both N-channel and P-channel devices to conduct, as with all CMOS devices. This gives rise to conduction path from V_{CC} to ground and will increase I_{CC} many orders of magnitude over its static level. Unused inputs should always be tied directly to the appropriate power rail, as a floating input will float to the input threshold, causing increased power dissipation.

Interfacing



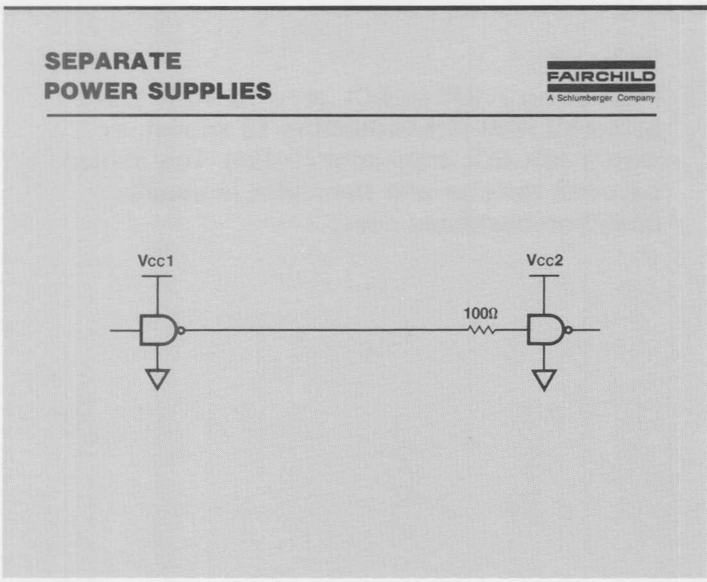
Slide 4.7
Interfacing FACT to ECL at −5.2 volts can be achieved with three resistors as shown, or with a 10K ECL translator (10124). The choice between resistor and translator is usually based on assembly costs.

Interfacing



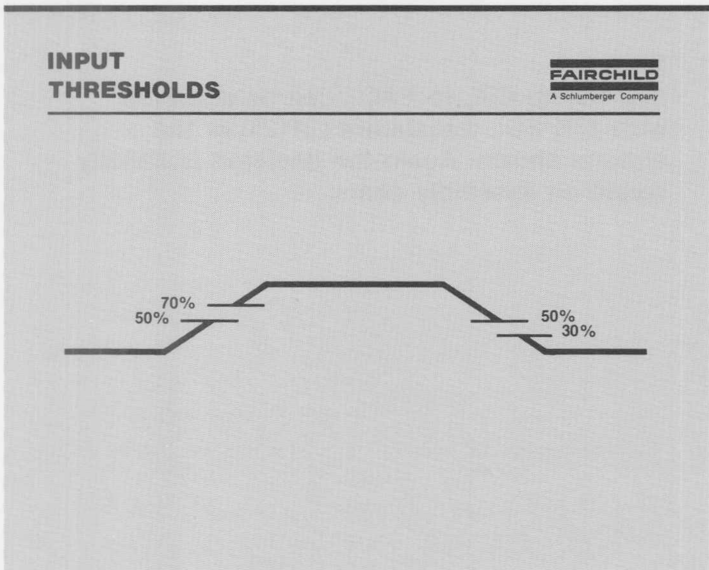
Slide 4.8
Interfacing ECL to FACT can be achieved with 10K ECL translators (10125) or the circuits shown. Again the decision is usually based on assembly costs.

Interfacing



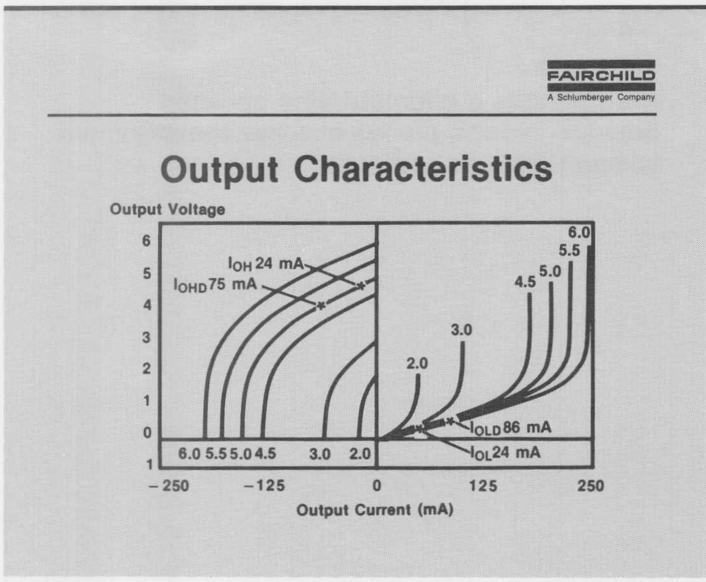
Slide 4.9
If separate or differing power supplies are used, interfacing is again quite easy. Some form of current limiting must be inserted in the signal line to limit current flow from V_{CC1} through the input clamp diodes to V_{CC2} when V_{CC2} is not present or of a substantially lower value than V_{CC1}. A resistor of 100 ohms is a good choice and can be placed at the driver to act as a line series termination.

Line Driving



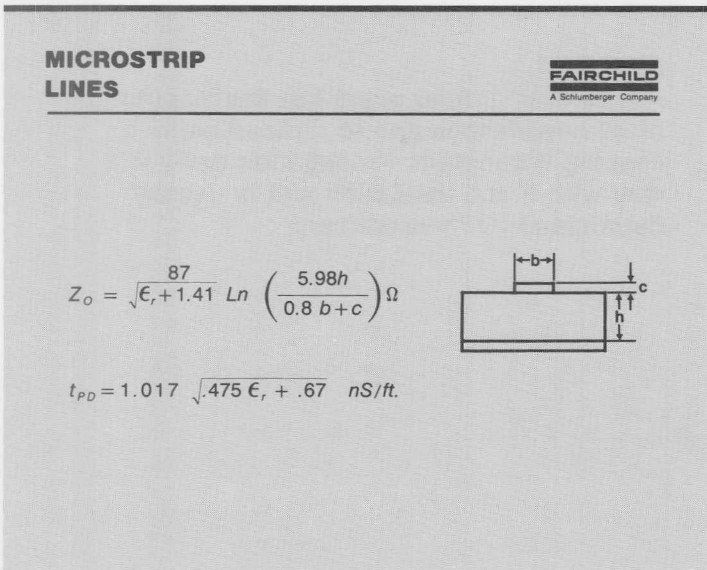
Slide 4.10
Efficient line driving requires that inputs switch on incident wave. This is the initial step voltage that propagates down a line before any reflections occur. FACT has its guaranteed input thesholds as 30 and 70% of V_{CC} respectively and switching typically occurs at 50% V_{CC}. These input thresholds give good noise immunity and minimize any double crossing of the input by a ringing wave front.

Line Driving



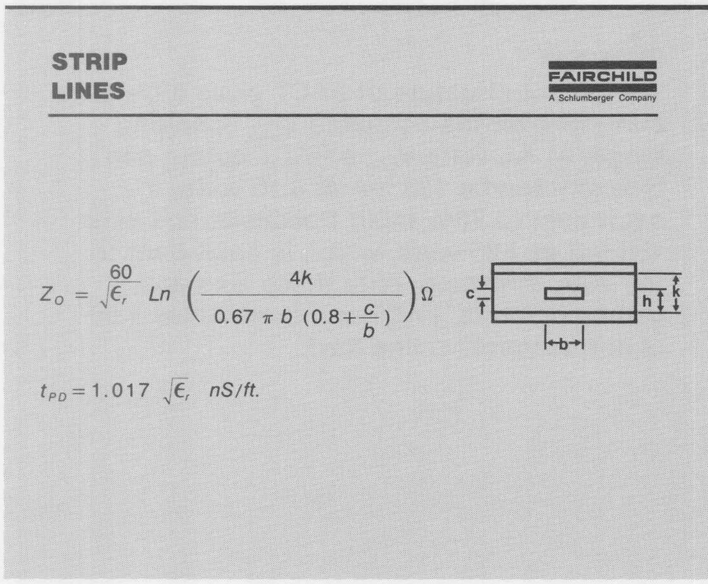
Slide 4.11
The output structure of FACT gives high drive currents over the complete V_{CC} operating range. At 4.5 volts V_{CC} a FACT output can typically source 130 mA at 3.15 volts, equivalent to 70% input threshold, and sink 150 mA at 1.35 volts, which is equivalent to the 30% threshold. With these sink and source currents, FACT can easily drive a 50 ohm transmission line load.

Line Driving



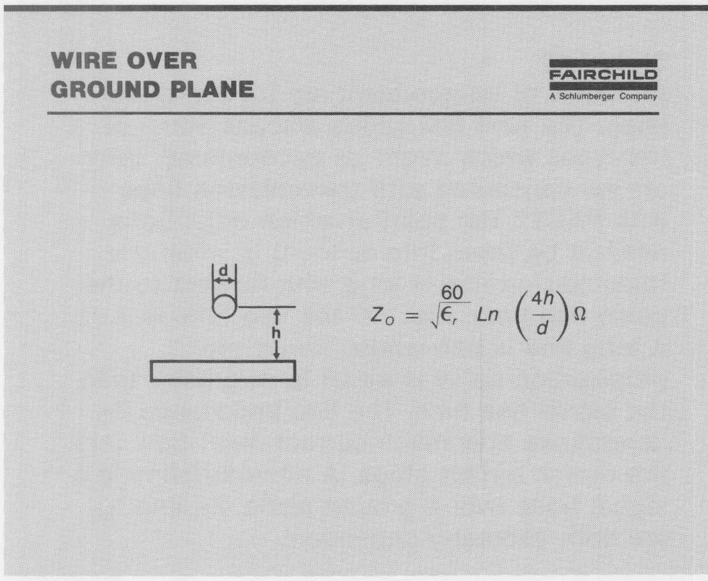
Slide 4.12
All forms of interconnect are transmission lines. The next few slides discuss some of the types which might be encountered. Why are we concerned with transmission lines with FACT? The point at which reflections need to be taken into account is when the transmission line is long with respect to the pulse rise time; with AC the rise time is 3 ns. A long line is one whose round trip propagation delay is equal to or greater than the signal rise time. The line impedance Z_O determines how much current must flow into the device output stage. A microstripline is a signal trace over a ground plane, Z_O and t_{pd} are both geometry dependent.

Line Driving

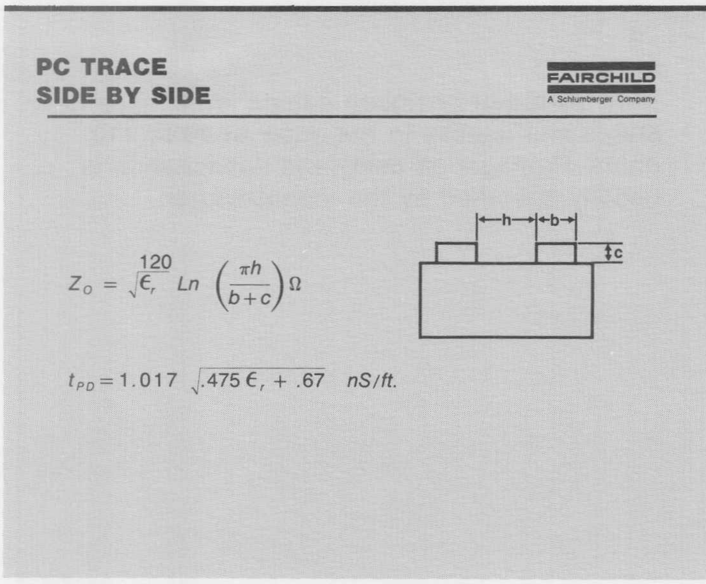


Slide 4.13
A stripline is a microstripline encased between ground planes and has the minimum susceptibility to crosstalk.

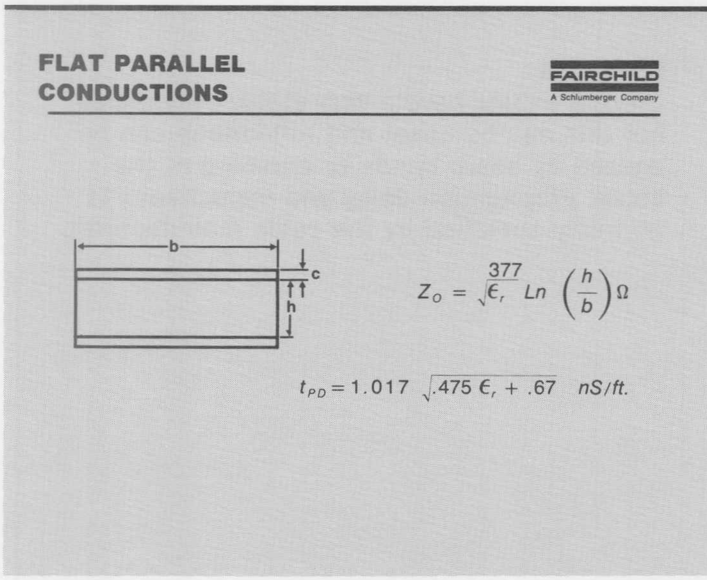
Line Driving



Slide 4.14
A wire over ground plane has the least stable of all impedances due to difficulties in keeping h constant. Propagation delay will vary with h and insulation and is usually determined by measurement.

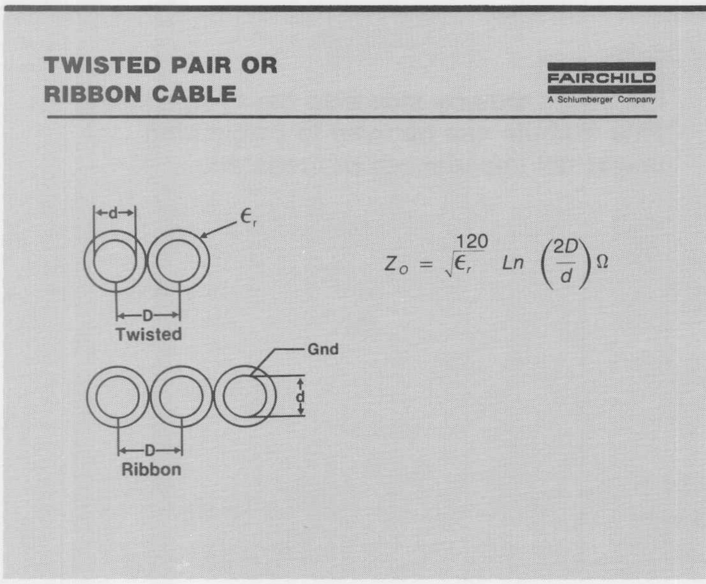


Slide 4.15
PC traces side by side also have impedance. This formula can be used in calculating power rail impedances or crosstalk.



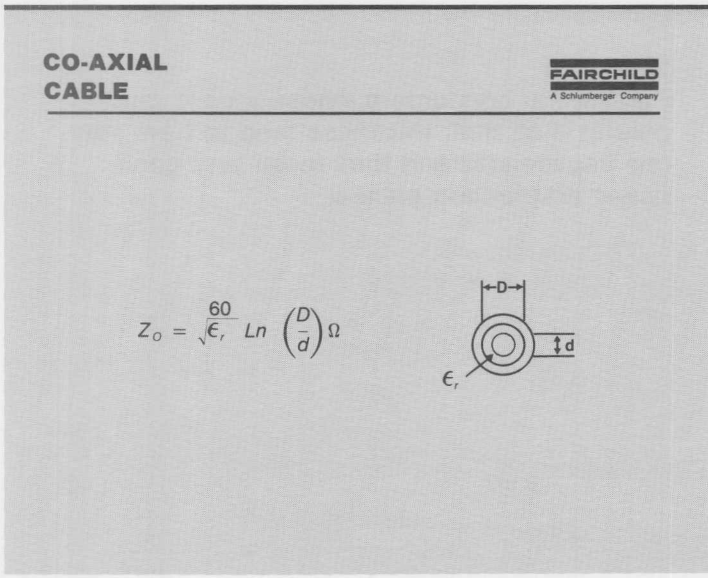
Slide 4.16
Parallel flat conductors whose area is much greater than their thickness tend to have very low impedances and thus make very good power distribution planes.

Line Driving



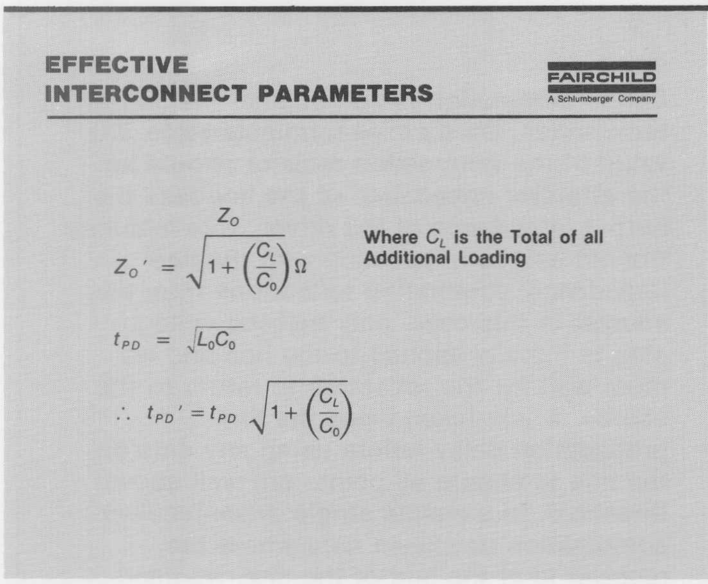
Slide 4.17
In twisted pair or ribbon cables impedance is stable and usually in the order of 70 to 110 ohms. Propagation delay and capacitance is usually specified by the manufacturer.

Line Driving



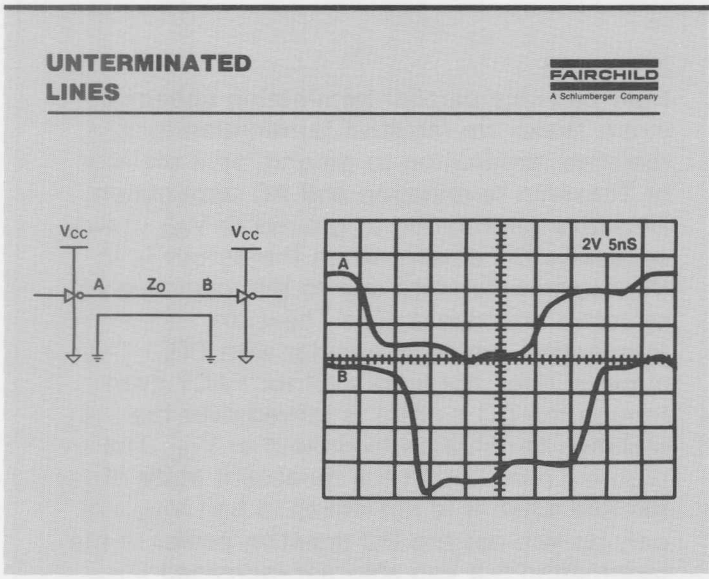
Slide 4.18
Coaxial cables have a very stable impedance but this can be upset and reflections can be caused by sharp bends or crushing of the cable. Propagation delay and capacitance is normally specified by the cable manufacturer.

Line Driving



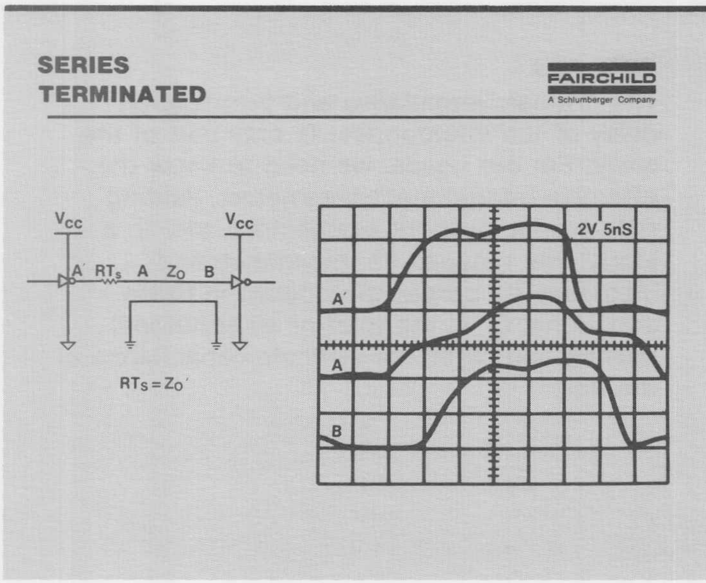
Slide 4.19
The intrinsic impedance and propagation delay of the interconnect is only part of the story. For our needs, we need to know the effective interconnect parameters. Adding gate inputs, outputs, connectors, etc. to a signal line reduces its impedance and increases its propagation delay. In these equations, C_L is the total of all additional loading and C_O is the intrinsic capacitance of the line.

Line Driving



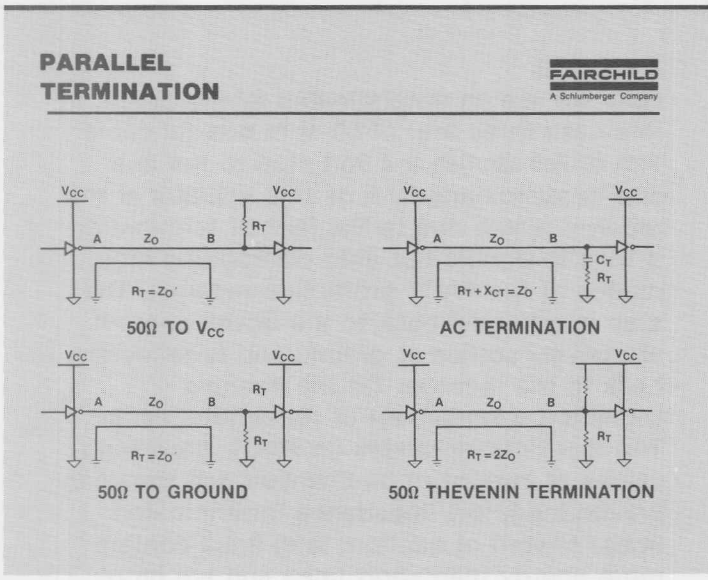
Slide 4.20
Here we see an unterminated interconnect, in this case three feet of 50 ohm coaxial cable. The driver applies a 4 volt step to the line and in approximately 5 ns this appears at the receiver where due to the lack of termination it tries to double but gets clamped by input diodes of the FACT protection network. The step is reflected back to the driver where it effectively settles at ground and is reflected back to the receiver. On the positive transition a similar set of reflections occur. The input clamp diodes on FACT allow high values of current to be clamped and thus can handle long, low impedance unterminated lines. A word of caution: long lines contain more energy than short lines and are more likely to give rise to crosstalk problems than terminated lines.

Line Driving



Slide 4.21
Series termination is one popular method of termination. On a series-terminated line, the value of the termination resistor should be the effective impedance of the line less the output impedance of the driver. This matches the net source impedance with the line impedance, eliminating reflections from the source. In this case, only half the voltage step is initially applied to the line and we must wait for the reflection to return to the source, which takes twice the line propagation delay before using any data on the line to ensure all points are well above threshold. In a simple single driver-receiver combination as shown here where the receiver is at the end of the line, we need only to wait for the line propagation delay before using the data. On a line where the receiver is between the driver and the end of the line, we must wait long enough for the initial wave front to reach the end of the line and the reflection to return to the receiver before we can use the data.

Line Driving



Slide 4.22
Four possible parallel termination schemes exist. These are resistive termination to V_{CC}, resistive termination to ground, split resistor or Thevenin termination and AC termination. Resistive termination to ground or V_{CC} draws excessive DC current when the output is in the appropriate state due to the low value of effective impedance. The Thevenin termination, which is popular with TTL circuits, does not work well for FACT even though the DC current is halved over the resistive termination to ground or V_{CC}. The problem here is that the quiescent state of the line when it is not driven is half V_{CC}, not only do you get the DC resistive power in the termination but you also get increased I_{CC} due to both transistors in the input causing simultaneous conduction of the input stage of the receiver.

Line Driving

AC TERMINATION

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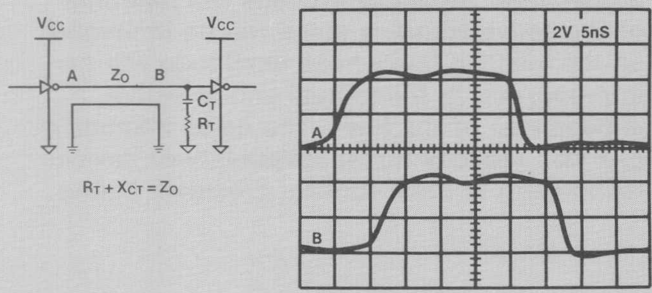

Slide 4.23
AC termination gives no DC current drain and terminates the line in its effective impedance. If used on a 3-state bus, the bus will remain in its last state for a few milliseconds. The AC termination is made up of a resistor and capacitor in series—the capacitor should have an X_C value of less than 5% of the effective impedance at a frequency of $\frac{1}{2}t_{pd}$ of the line, irrespective of pulse repetition rate. A 10 nF decoupling capacitor works well in these circumstances, being both low cost and readily available. A 10 nF capacitor will have an X_C of approximately 100 mΩ for a line propagation delay of 10 ns, so R_S should be the same value as the line impedance.

Crosstalk

CROSSTALK

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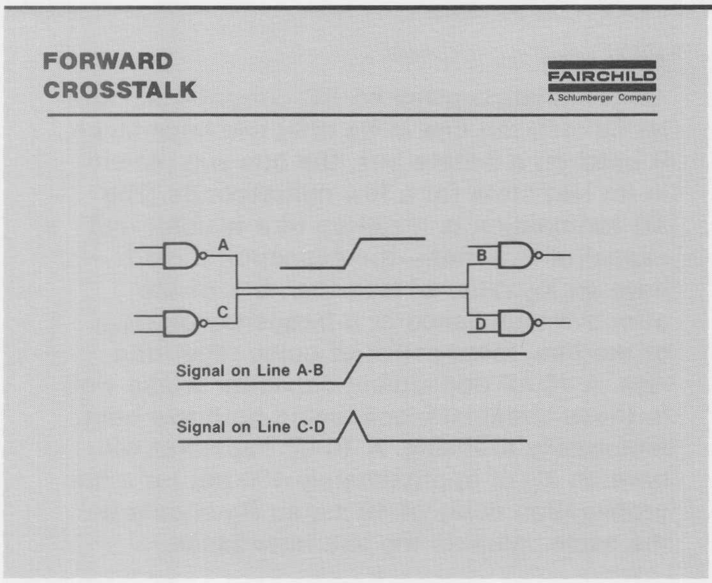
- Forward Crosstalk
  Coincident with Wave Front on Active Line
  Exists for Duration of Wave Transmission
- Reverse or Backward Crosstalk
  Flows Away from Wave Front on Active Line
  Exists for Twice Line Propagation Delay
- Both Causes Problems
  Extent and Nature are Circuit Dependent

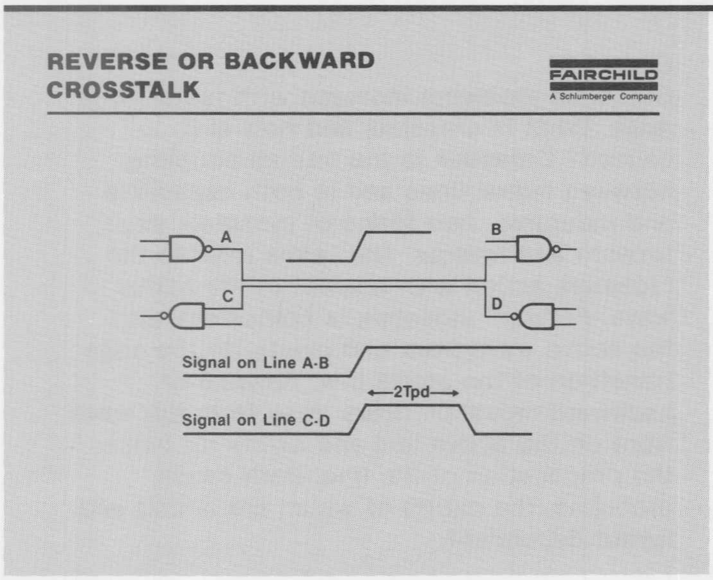
Slide 4.24
Crosstalk problems increase with faster edge rates. What is crosstalk and how is it caused? Crosstalk is the mutual coupling between signal lines and is both capacitive and inductive. Two forms of crosstalk exist, forward and reverse. The terms refer to the crosstalk action with respect to the active wave. Forward crosstalk is coincident with the active wave front and exists for the edge transition of the active line. Reverse or backward crosstalk flows away from the wave front on the active line and exists for twice the propagation of the line. Both cause problems, the nature of which are circuit and layout dependent.

Crosstalk



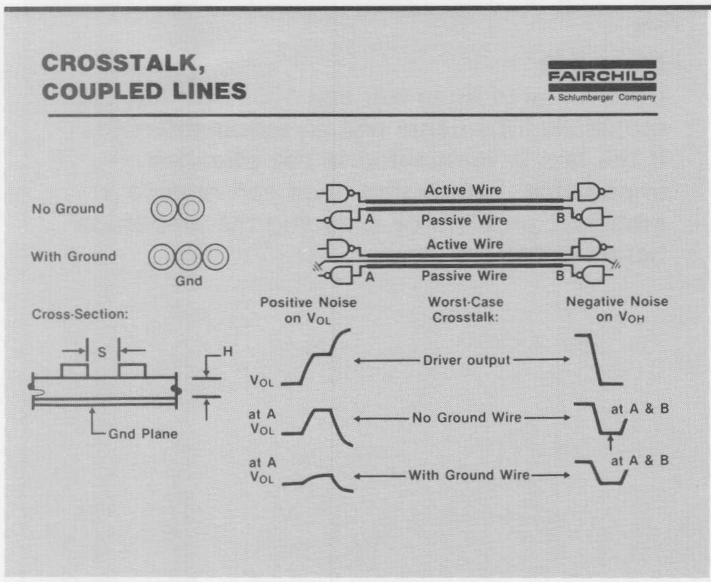
Slide 4.25
Due to the close proximity of signal lines A-B and C-D, mutual coupling exists. If the length of the coupled section is such that its propagation equals or exceeds the rise time of the active signal, a pulse will be impressed on the inactive line whose amplitude will be in proportion to the mutual and effective impedances of the lines. The noise immunity of FACT reduces the susceptibility of devices responding to most forward crosstalk pulses.

Crosstalk



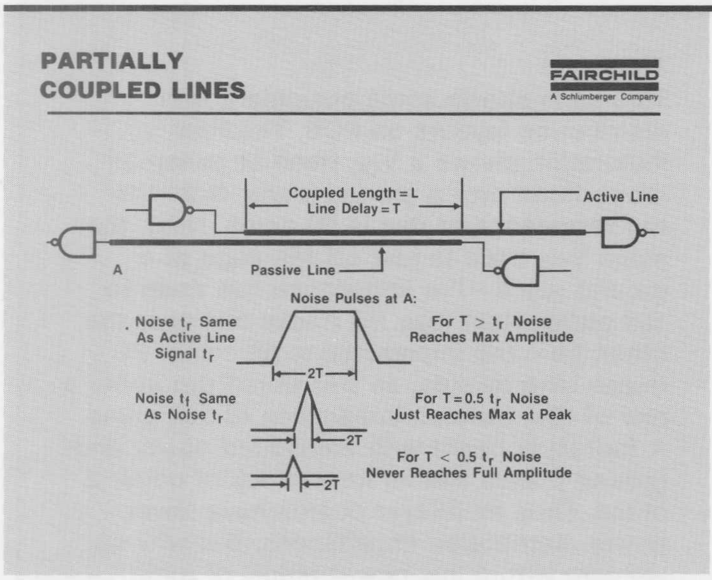
Slide 4.26
Reverse crosstalk can be a major problem in the case shown here, where the propagation delay of the coupled section of line is many times larger than the signal rise time. The crosstalk pulse will exist for twice the propagation delay of the line. This kind of problem is one of the most difficult to cure, but we will see some cures later.

Crosstalk



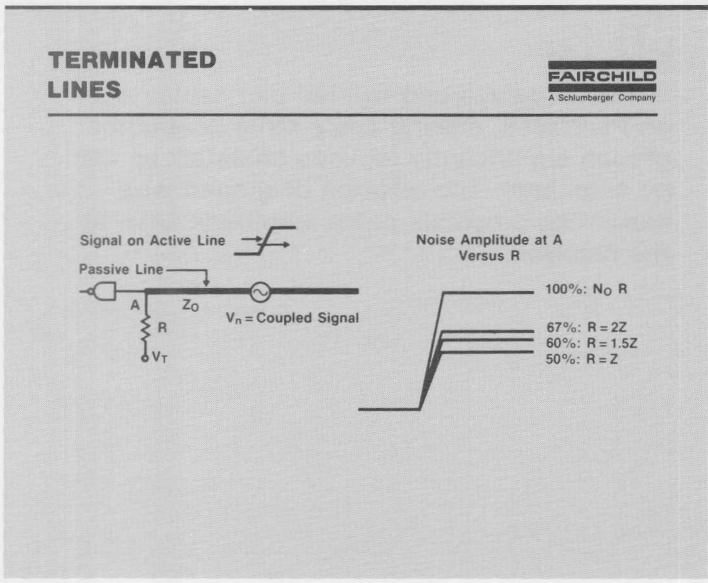
Slide 4.27
In ribbon cables and twisted pair cables and on PC traces, making every other conductor ground significantly reduces crosstalk as can be seen here. The addition of ground wire halves the crosstalk pulse amplitude seen at the receiver.

Crosstalk



Slide 4.28
With partially coupled lines the crosstalk is maximum when the line delay is much larger than the active signal rise time. If the length of the coupled line delay is equal to the rise time, then the crosstalk is a pulse whose amplitude just reaches maximum. When the coupled length delay is less than the active rise time, the crosstalk pulse never reaches full amplitude and can be rejected by the receiving FACT gate. For FACT, coupled lines on printed circuit boards should be kept under 12 inches.

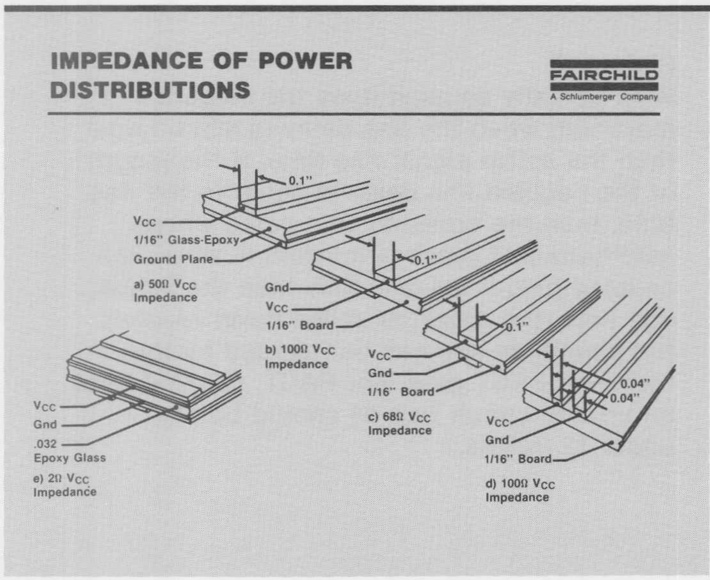
Crosstalk



Slide 4.29

Unterminated lines will see 100% of induced crosstalk. This value will be reduced to 50% if the line is terminated in the effective impedance. Terminated lines can remove a crosstalk problem by reducing the amplitude below threshold levels.

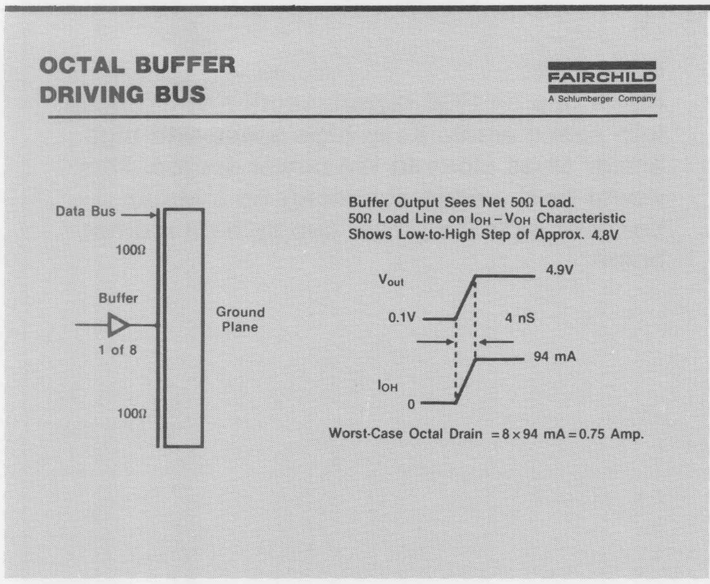
Decoupling



Slide 4.30

This slide shows some possible power distribution layouts on PCB. The first illustration shows a V_{CC} trace of generous proportions over a ground plane. Note that the impedance of this is 50 ohms. Next, the same V_{CC} trace is just off the edge of a ground plane—the impedance has risen to 100 ohms. Next, two PC traces one over the other, here the impedance is 68 ohms. PC traces side by side, as you would run under a row of ICs, have an impedance of 100 ohms. A four-layer board with embedded power and ground planes has an impedance of under 2 ohms. Thus multilayer boards have lower power distribution impedances. But why do we care with a low power family of logic devices?

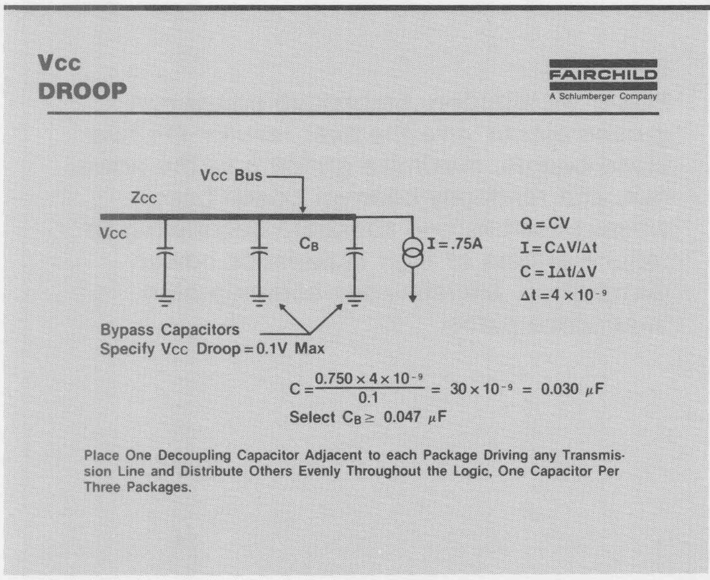
Decoupling



Slide 4.31

Consider the octal buffer driving a 100 ohm bus. Part way along the line the buffer will see two 100 ohm stubs in parallel, making a net 50 ohm load. This buffer will switch between the rails, demanding over 90 mA per output. If all outputs are switching, this would add up to .75 A of current to be supplied by the power supply. The impedance of the power distribution is in series with the device and a voltage drop will occur across the impedance, reducing the output swing to the device.

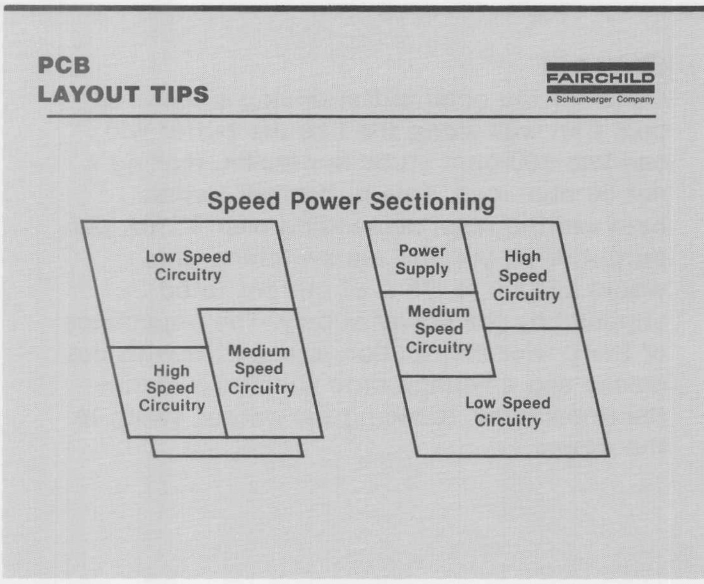
Decoupling



Slide 4.32

To reduce the voltage droop at the device, we use decoupling capacitors local to the device to supply the transient power to the driver. The value of the decoupling capacitor can be determined from the formula shown. Good design practice is to place a decoupling capacitor adjacent to any package driving a transmission line and distribute others evenly throughout the logic, one capacitor for every three packages.

PCB Layout



Slide 4.33
Some tips on PCB layout: section your design into speed areas. Keep high speed and high power areas close to the power source. This would be the edge connector on a plugin board or near the power supply on a mother board.

PCB Layout

PCB LAYOUT TIPS

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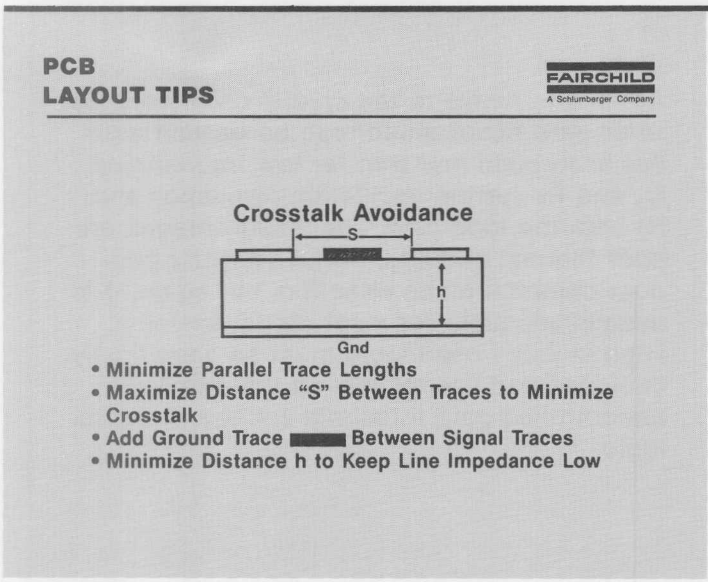
Power Distribution

- Embedded Power and Ground Planes Give Best Results
- On 2 Sided Boards Maximize Gridding of Power Bus and Randomly Interconnect Power Busses Where Possible
- Use Adequate Decoupling to Reduce Effects of High Z Power Distribution
- Minimize High Impedance Common Paths

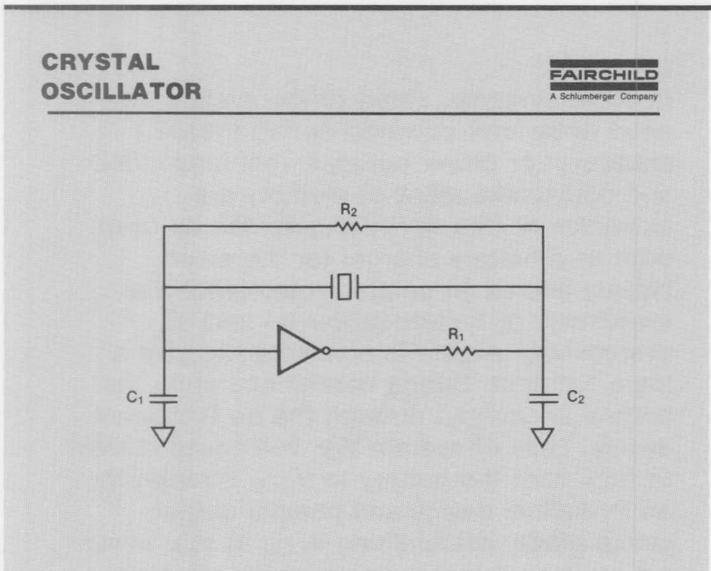
Slide 4.34
Power distribution. Embedded power and ground planes give the best results. On two-sided boards, maximize gridding of the power bus, and randomly connect power buses where possible. Use adequate decoupling to reduce effects of high impedance power distribution. Minimize any common high impedance paths.

PCB Layout



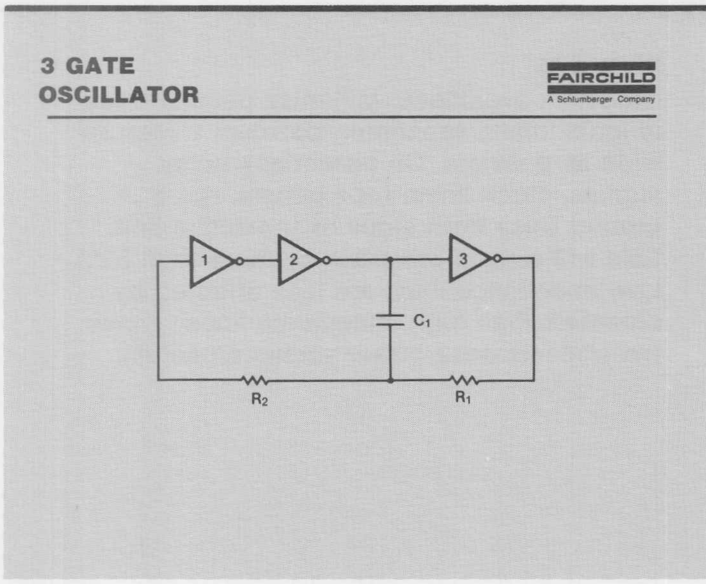
Slide 4.35
Crosstalk avoidance. Minimize parallel trace lengths, make separation between traces as wide as possible. On potentially noisy signals, clock lines, for example, run a ground trace both sides of the active line. This will reduce crosstalk by more than 50%. Low impedance lines are less affected by crosstalk than high impedance lines—make the tradeoff drive power versus crosstalk.

Oscillators



Slide 4.36
Most systems require fixed frequency oscillators. The single inverter crystal oscillator shown performs well for this type of circuit and starts reliably. In this circuit, C_1 and C_2 match the C_s of the crystal, R_1 limits the drive into the crystal to avoid overload, R_2 establishes DC conditions for the loop, biasing the input stage to close the switching threshold. The disadvantages of this type of circuit are poor thermal and long term stability, frequency jitter and poor common mode rejection. Having said all that, however, it is usually adequate for most digital systems.

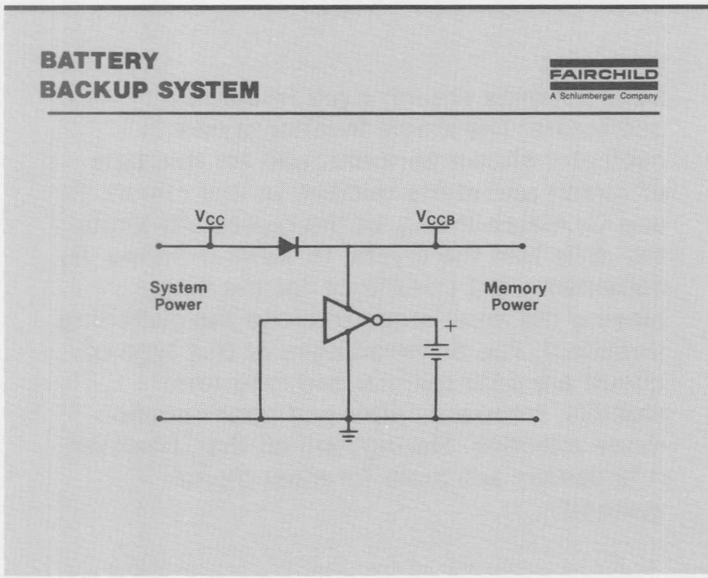
Oscillators



Slide 4.37

As an alternative to the crystal oscillator, the three-gate RC oscillator can be used. This is easier to build and trim for low frequencies, C_1 and R_1 set the oscillation frequency and R_2 sets the loop gain. The disadvantages are poor thermal stability, frequency jitter and poor common mode rejection, but again, it is usually adequate for most digital systems. High stability oscillators must be specifically designed and cannot rely on the relatively uncontrolled gate threshold voltage of digital logic.

Battery Backup



Slide 4.38

In some systems, a part of the system may need to be kept powered during system shutdown or power outages; real time clock and nonvolatile areas of memory are examples of this. A FACT gate can be used both as a battery charger for the nicad battery and as an uninterrupted glitchless switchover to battery power on loss of system V_{CC}. A gate is connected to give a logic 1 output. During normal operation the battery is charged through the on P-channel device. Loss of system V_{CC} will cause current to flow from the battery to V_{CCB} through the on P-channel device and parallel output clamp diode, establishing V_{CCB} at V_{BAT} minus a diode drop. It is recommended that current to V_{CCB} be limited to 85 mA per output, additional gates may be paralleled to achieve higher output currents.

Memory Board Design

MEMORY READ TIMING

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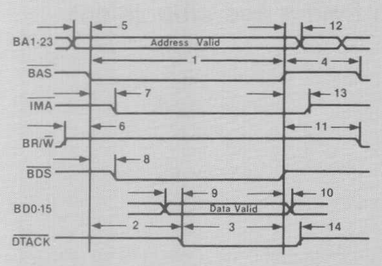

Read Cycle Timing		Performance		Requirements	
Label	Parameter	Min	Max	Min	Max
2	BAS Low to DTACK Low		272		1500
3	DTACK Low to BAS High	0			350
4	BAS High	100		140	
5	Address Setup Before BAS Low	10		15	
6	BR/W High to BAS Low or BDS Low	10		15	
7	BAS Low to IMA Low		55	0	70
9	Data Setup Before DTACK Low	63		55	
10	Data Hold After BAS or BDS High	24	45	0	100
11	BR/W Hold After BAS or BDS High	50		65	
12	Address Hold After BAS or BDS High	0		15	
13	BAS High to IMA Release	18	34		50
14	BAS High to DTACK Release	18	34		50

Slide 4.39
Memory board design. The next few slides will demonstrate techniques used in designing a battery backup memory board design. It will also illustrate the power saving benefits of FACT technology at the system level. The design uses AC, ACT and the Fairchild F1601 64K static CMOS RAMs on a battery backup 256K byte board. The host computer is the HP 9000 series computer, with an 8 MHz 68010 processor. Let's start with the system requirements: this first slide shows the bus timing for a memory read cycle, processor or DMA—you can see that the board has been designed to perform a read cycle in 272 ns using 70 ns access RAMs, which is the system requirement and is processor limited.

Memory Board Design

MEMORY WRITE TIMING

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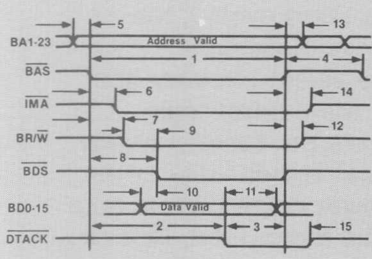
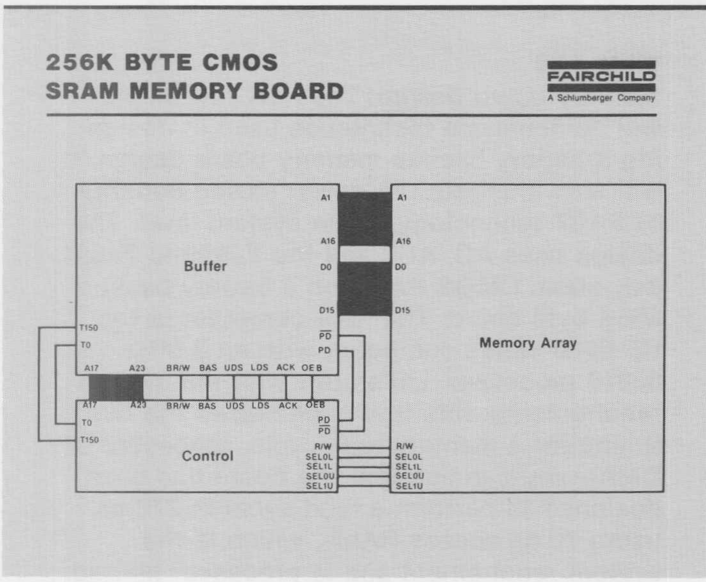


Write Cycle Timing		Performance		Requirements		Notes
Label	Parameter	Min	Max	Min	Max	
1	BAS Low to DTACK Low	180				1
2	BDS Low to DTACK Low		210		1500	2
5	Address Setup Before BAS Low	10		15		
6	BAS Low to IMA Low	32	55	0	70	
7	BAS Low to BR/W Low		100	75	45	
9	BR/W Low to BDS Low	10		65		
10	Data Setup Before BDS Low	0		15		
11	Data Hold After DTACK Low	30		85		
12	BR/W Hold After BAS or BDS High	0		15		
13	Address Hold After BAS or BDS High	0		15		
14	BAS High to IMS Release	18	34	0	50	
15	BAS High to DTACK Release	18	34	0	50	

Notes: 1 When BDS Low Before BAS Low
2 When BAS Low Before BDS Low

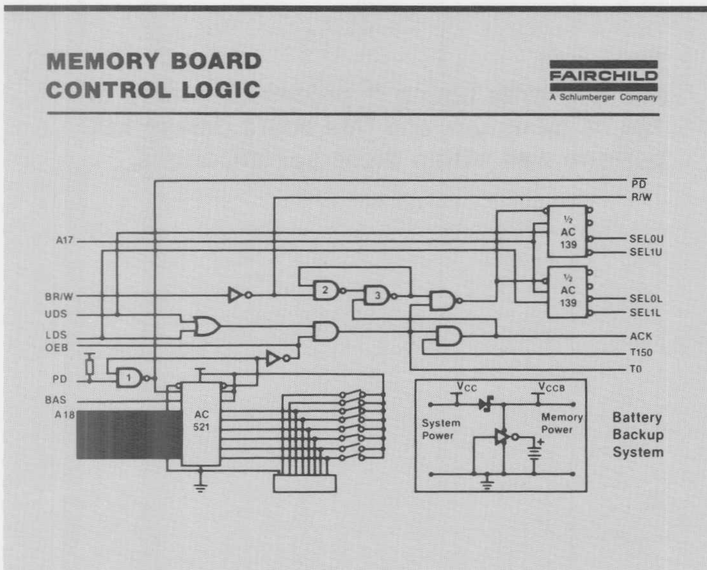
Slide 4.40
Memory write timing is processor limited to 180 ns minimum, and this board design will perform well within these specifications.

Memory Board Design

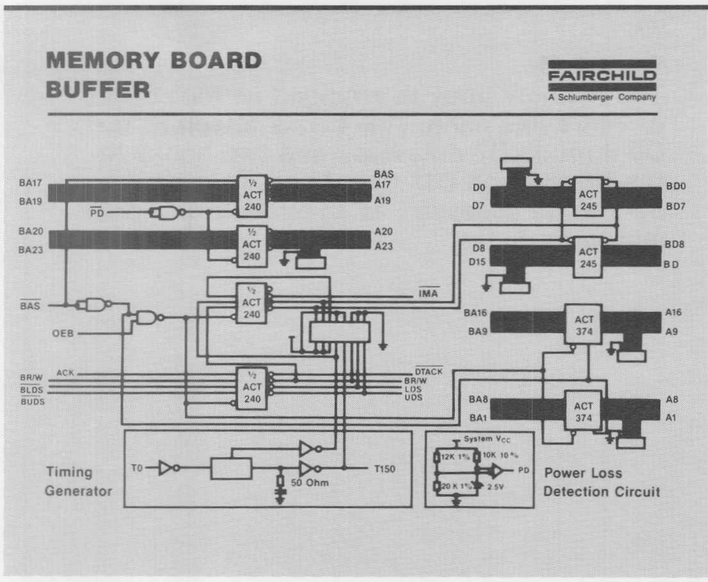


Slide 4.41
The design is split into three logical areas: memory array containing 32 64K static RAMs, the buffer area handling interfacing to system bus and driving the array, and the control section generating all timing and chip select signals.

Memory Board Design



Slide 4.42
The control logic section receives buffered signals from the bus via the buffer section and contains the board address decoder (the 'AC521), the interlock circuitry to ensure that the memory never gets short cycled, the battery backup system as discussed previously and the chip select circuitry (the 'AC139). All devices in the control logic section are powered from the battery supply. This ensures that critical signals stay in the correct state during power down. Let us take a minute and look at the logic. First, look at NAND gate #1. This is here to lock out the power down signal, P_D, whenever the 'AC521's equality signal is active. This NAND gate also performs a second function—once the P_D signal has gone active, it will lock out any further memory cycles until the P_D signal is released. This gate ensures that 1) a memory cycle is not cut short when the power falls off, and 2) that once power is lost, any spurious glitches on the system buses will not corrupt the stored data.



Slide 4.43

The buffer section interfaces to the TTL system bus with ACT devices to ensure logic swing compatibility. The address lines to the memory array are latched using the 'ACT374 to minimize logic level changes in the memory array, which cause increased power consumption and 3-stated when the board is inactive, reducing power consumption to a minimum. The 'ACT374 directly drives the memory array via series terminating resistors to optimize wave shape due to the high capacitive loading of the bus. All of the buffers except the 'ACT241 driving the high address bits are 3-stated when the board is not addressed. This is done to eliminate any system bus glitches onto the board. The high address lines are not 3-stated, except during power loss, to minimize the board response time. All signal lines feeding the control section or the memory array have pulldown resistors fitted to ensure these lines are pulled to ground during non-operation or power down stages. Notice that the buffer enable signal, OEB, is gated with BAS. This is done to insure that the handshake lines, DTACK and IMA, are released within 50 ns of the board being deselected. An LC delay line is used to generate acknowledge timing and data bus control signals, which further reduces power consumption by eliminating bus contention problems. A power loss detection circuit informs the control logic when system V_{CC} is below usable limits, ensuring erroneous memory accesses are not performed during power up or power loss phases. All devices in the buffer section are system V_{CC} powered, which keeps the standby current to a minimum.

Memory Board Design

MEMORY ARRAY

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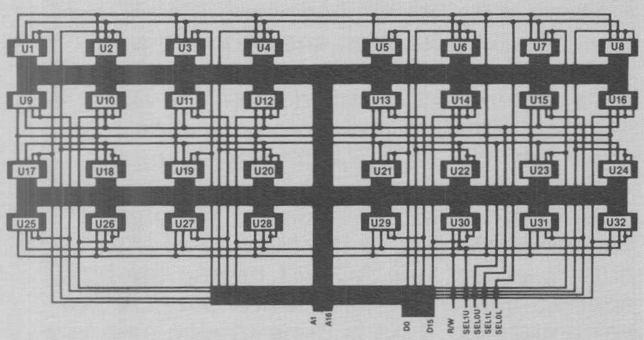

Slide 4.44
The memory array is arranged as four banks of 64K bytes each. Two banks attach to the D0 through D7 data lines and two banks to the D8 through D15 data lines. This allows data to be accessed as 16-bit word or upper and lower bytes.

Memory Board Design

BATTERY BACKUP
SPECIAL CONSIDERATIONS

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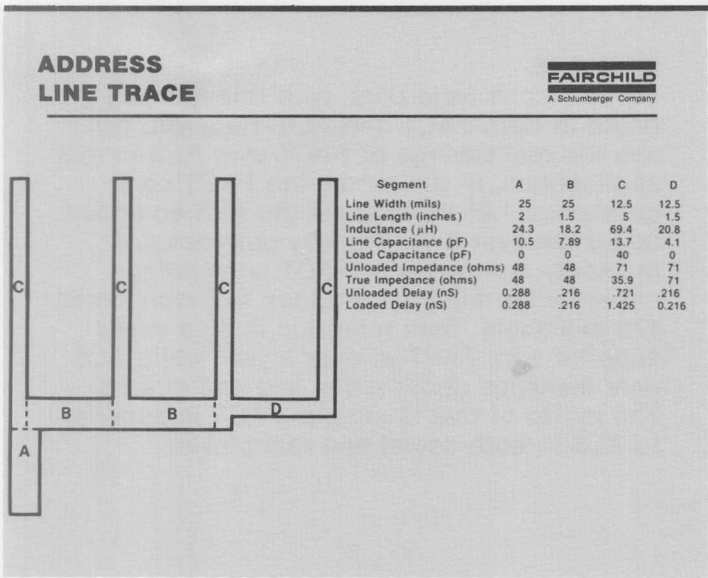
- All I/O Between the System and the Board Must Be Buffered with 3 State Buffers to Eliminate any Power Flow from the Battery when the System is Powered Down.
- All Inputs from the System Must Be 3-Stated During Power Loss.
- All Outputs from the Board Must Be Active Low Signals to Eliminate Current Flow Through Parasitic Diodes During Power Loss.
- All Inputs to Onboard Chips Must Be Driven to within 0.2V of a Power Rail.
- The Power Loss Detection Circuit Should Not Terminate an Active Memory Cycle if the Board is Addressed.

Slide 4.45
Notes.

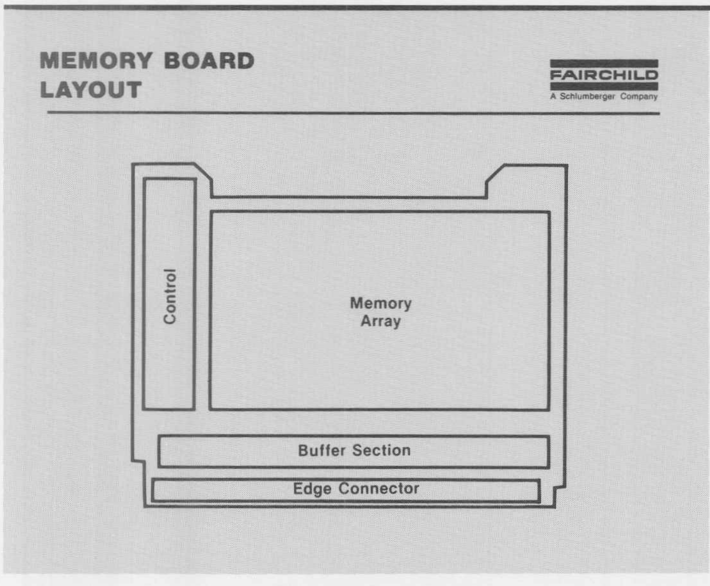
Memory Board Design



Segment	A	B	C	D
Line Width (mils)	25	25	12.5	12.5
Line Length (inches)	2	1.5	5	1.5
Inductance (μH)	24.3	18.2	69.4	20.8
Line Capacitance (pF)	10.5	7.89	13.7	4.1
Load Capacitance (pF)	0	0	40	0
Unloaded Impedance (ohms)	48	48	71	71
True Impedance (ohms)	48	48	35.9	71
Unloaded Delay (nS)	0.288	.216	.721	.216
Loaded Delay (nS)	0.288	.216	1.425	0.216

Slide 4.46
Now that we have finished the board design and layout, we need to consider terminations. The memory array address trace has the most heavily loaded lines, each one with 32 inputs loading it. It is here we should examine the need for terminations. The board used is a four-layer board with center layers used for power and ground. Here is the address trace, which shows four stubs, each running up one bank of memory chips. When the trace shown was evaluated, it was found that a 33 ohm resistor series termination optimized the signals throughout the memory array by closely matching the source impedance with the loaded line impedance. This value minimized the noise spikes on the trace and maximized the amplitude of the initial signal generated on the line. For your information, we have listed all of the pertinent data. The data shows all loaded and unloaded trace inductances, capacitances and delays.

Memory Board Design



Slide 4.47
The memory board layout fits the 6.5 x 4.5 inch board well with each section easily identified. As can be expected, the memory array occupies the largest board area.

Memory Board Design

ACMOS POWER VS ALS POWER
CMOS 256KBYTE SRAM BOARD

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ACMOS		ALS	
Run	Stdby	Run	Stdby
1.95 W	440 μW	3.03 W	170 mW

Battery Life in Standby Mode
Battery = NiCad Cell Rate @ 1 Ahr

ACMOS	ALS
11,360 hr (1.14 yr)	29.4 hr

Slide 4.48
Comparisons were done with this memory board in both FACT and ALS. Here you can see the real savings of FACT over ALS in real applications. In run mode, the FACT card consumed 1.95 W whereas the ALS equipped board ran over 3 W. Standby currents are markedly reduced with FACT consuming under half a milliwatt whereas ALS consumed 170 milliwatts. Data retention is also vastly superior with FACT at over a year while ALS only manages under a day and one quarter. The motto of this is simple: FACT is superior to ALS in both speed and real power.

Part Type and Function

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Flip-Flops

Function	Device	3-State Outputs	Master Reset
Dual D	54AC/74AC74	No	No
Dual JK̄	54AC/74AC109	No	No
Quad D Flip-Flop	54AC/74AC175	No	Yes
Quad D Flip-Flop	54AC/74AC379	No	No
Hex D Flip-Flop	54AC/74AC174	No	Yes
Octal D Flip-Flop	54AC/74AC273	No	Yes
Hex D Flip-Flop	54AC/74AC378	No	No
Octal D Flip-Flop	54AC/74AC374	Yes	No
Octal D Flip-Flop	54AC/74AC377	No	No
Octal D Flip-Flop	54ACT/74ACT374	Yes	No
Octal D Flip-Flop	54AC/74AC564	Yes	No
Octal D Flip-Flop	54ACT/74ACT564	Yes	No
Octal D Flip-Flop	54AC/74AC574	Yes	No
Octal D Flip-Flop	54ACT/74ACT574	Yes	No

Slide 5.5
Dual JK and D-type flip-flops in quad, hex, and octal configurations are offered in industry standard and broadside pinouts. All flip-flops operate in excess of 75 megahertz.

Part Type and Function

FAIRCHILD
A Schlumberger Company

Latches

Function	Device	3-State Outputs	Broadside Pinout
Octal D Latch	54AC/74AC373	Yes	No
Octal D Latch	54ACT/74ACT373	Yes	No
Octal D Latch	54AC/74AC563	Yes	Yes
Octal D Latch	54AC/74AC573	Yes	Yes
Octal D Latch	54ACT/74ACT563	Yes	Yes
Octal D Latch	54ACT/74ACT573	Yes	Yes

Slide 5.7
Octal latches, most with 3-state outputs, are available with standard and broadside pinouts operating with minimum propagation delay.

Part Type and Function

FAIRCHILD
A Schlumberger Company

Counters

Function	Device	Parallel Entry	Reset	U/D	3-State Outputs
4-Bit BCD Decade	54AC/74AC160	S	A	No	No
4-Bit Binary	54AC/74AC161	S	A	No	No
4-Bit Binary	54AC/74AC163	S	S	No	No
4-Bit Binary	54AC/74AC169	S	S/A	Yes	No
4-Bit Binary	54AC/74AC191	A	No	Yes	No
4-Bit Binary	54AC/74AC569	S	S/A	Yes	Yes

S = Synchronous
A = Asynchronous

Slide 5.8
The FACT family of high-speed 4-bit binary and BCD counters offers operational frequencies of 70 megahertz and greater.

Part Type and Function

FAIRCHILD
A Schlumberger Company

Shift Registers

Function	Device	No. Of Bits	Reset	Serial Inputs	3-State Outputs
Octal Shift/Storage Register	54AC/74AC299	8	A	2	Yes
Octal Shift/Storage Register	54AC/74AC323	8	S	2	Yes

S = Synchronous
A = Asynchronous

Slide 5.9
8-bit octal shift/storage registers with bi-directional I/O operate at frequencies typically above 75 megahertz.

Part Type and Function

FAIRCHILD
A Schlumberger Company

Buffers / Line Drivers

Function	Device	Enable Inputs (Level)	Inverting/ Noninverting	Broadside Pinout
Octal Buffer/Line Driver	54AC/74AC240	2(L)	I	
Octal Buffer/Line Driver	54ACT/74ACT240	2(L)	I	
Octal Buffer/Line Driver	54AC/74AC241	1(L) & 1(H)	N	
Octal Buffer/Line Driver	54ACT/74ACT241	1(L) & 1(H)	N	
Octal Buffer/Line Driver	54AC/74AC244	2(L)	N	
Octal Buffer/Line Driver	54ACT/74ACT244	2(L)	N	
Octal Buffer/Line Driver	54AC/74AC540	2(L)	I	Yes
Octal Buffer/Line Driver	54AC/74AC541	1(L) & 1(H)	N	Yes

Slide 5.10
All popular industry pinout buffers and line drivers are available with minimum propagation delays. These and all other FACT SSI/MSI devices have an output drive of ±24 milliamps, and are capable of directly driving 50 ohm impedance transmission lines.

Part Type and Function

FAIRCHILD
A Schlumberger Company

Multiplexers

Function	Device	Enable Inputs (Level)	3-State Outputs	Complementary
8-Input	54AC/74AC151	1(L)	Yes	Yes
Dual 4-Input	54AC/74AC153	2(L)	Yes	No
Quad 2-Input	54AC/74AC157	1(L)	Yes	No
Quad 2-input	54AC/74AC158	1(L)	No	Yes
8-Input	54AC/74AC251	1(L)	Yes	Yes
Dual 4-Input	54AC/74AC253	2(L)	Yes	No
Quad 2-Input	54AC/74AC257	1(L)	Yes	No
Quad 2-Input	54AC/74AC258	1(L)	No	Yes

Slide 5.12
The popular 2, 4, and 8-input multiplexers with standard and 3-state outputs offer high system performance with low power consumption.

Part Type and Function

FAIRCHILD
A Schlumberger Company

Decoders/Demultiplexers

Function	Device	LOW Enable	Active-HIGH Enable	Active-LOW Outputs	Active-Address Inputs
1-of-8 Decoder/Demultiplexer	54AC/74AC138	2	1	8	3
1-of-8 Decoder/Demultiplexer	54ACT/74ACT138	2	1	8	3
Dual 1-of-4 Decoder	54AC/74AC139	1 & 1	No	4 & 4	2 & 2

Slide 5.13
Industry standard 138 and 139 decoder/demultiplexers are available with CMOS or TTL compatible inputs.

Part Type and Function

FAIRCHILD
A Schlumberger Company

Comparators

Function	Device	Features
Octal Comparator	54AC/74AC520	Expandable/Pullup Resistors
Octal Comparator	54AC/74AC521	Expandable

Slide 5.14
Expandable octal identity comparators with optional pull up resistors on Q inputs simplify system address decoding logic.

Part Type and Function

FAIRCHILD
A Schlumberger Company

Transceivers/Registered Transceivers

Function	Device	Registered	Enable Inputs (Level)	3-State
Octal Bus Transceiver	54AC/74AC245	No	1(L)	Yes
Octal Bus Transceiver	54ACT/74ACT245	No	1(L)	Yes
Octal Bus Transceiver	54AC/74AC646	Yes	1(L) & 1(H)	Yes
Octal Bus Transceiver	54AC/74AC648	Yes	1(L) & 1(H)	Yes

Slide 5.15
The 'AC245 transceiver is available with CMOS and TTL compatible inputs. The registered octal transceivers 'AC646 and 648 give improved system performance with reduced package count.

Part Type and Function

FAIRCHILD
A Schlumberger Company

FIFOs

Function	Device	Input	Output	3-State Output
64 X 9 FIFO	54AC/74AC708	Parallel	Parallel	Yes
64 X 9 FIFO	54ACT/74ACT708	Parallel	Parallel	Yes

Slide 5.17
In addition to its SSI and MSI products, Fairchild also offers high performance CMOS LSI devices for use in state-of-the-art applications.

The FACT family of 64x9 FIFOs with both CMOS and TTL input options feature zero fall through time. The 'ACT708 provides full, empty, and half full status lines, and is cascadeable to increase stack width and depth without the use of additional interface logic.

Part Type and Function

FAIRCHILD
A Schlumberger Company

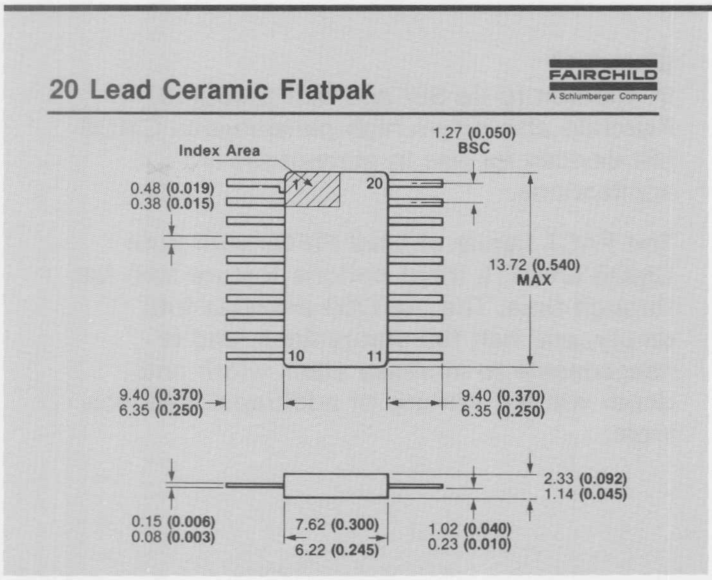
Arithmetic Functions

Function	Device	Features
16X16 Multiplier/Accumulator	54AC/74AC1010	2's Complement & unsigned arith.
16X16 Multiplier/Accumulator	54ACT/74ACT1010	2's Complement & unsigned arith.
16X16 Multiplier	54AC/74AC1016	2's Complement & unsigned arith.
16X16 Multiplier	54ACT/74ACT1016	2's Complement & unsigned arith.
16X16 Multiplier	54AC/74AC1017	Common Clock
16X16 Multiplier	54ACT/74ACT1017	Common Clock
DSP ALU	54AC/74AC705	8 Arith/Logic Functions

Slide 5.20
High performance 16-bit multipliers with 2s complement, unsigned arithmetic and mixed mode multiplication have 40 nanosecond multiply cycle times. These devices, which feature 3-state outputs and are pin compatible with TRW's MPY-16 multiplier, are especially useful in FFT, video and array processors.

The 'ACT705 is another device in our expanding line of FACT LSI products. This ALU, which is especially designed for digital signal processing, features 50 nanosecond cycle times, performs 8 arithmetic and logic functions and has a multiplier/accumulator with a 16-bit product output. The 'AC705 can be used in edge enhancement, spatial filtering and feature extraction applications.

Packages and Packaging



20 Lead Ceramic Flatpak
Packaging has been developed through the years to keep pace with the requirement for higher integration on silicon. As the scales of integration on silicon increase, packaging techniques must change to accommodate larger die sizes and increasing pinouts.

With the advent of RTL and CTL type logic, the Flatpak was devised...the first real digital package. This package was expensive to manufacture and difficult to mount or service.

Packages and Packaging

20 Lead Ceramic Dual In-Line

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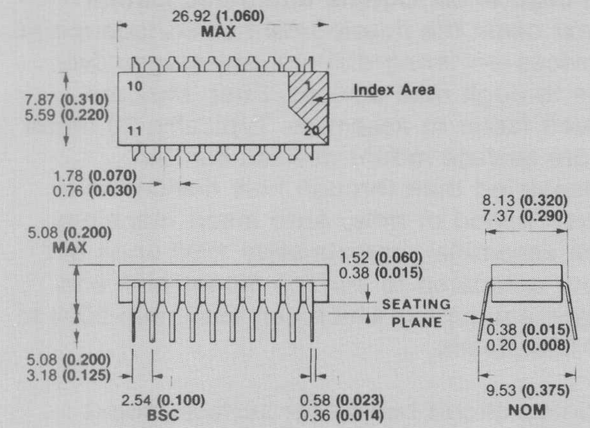
A Schlumberger Company



20 Lead Ceramic Dual In-Line
The Dual In-Line package was then developed as a cost effective alternative. Ceramic devices came first which utilized the through hole mounting technique. Ceramic DIPs were much easier to mount than Flatpaks, reducing assembly time and costs.

Packages and Packaging

20 Lead Plastic Dual In-Line

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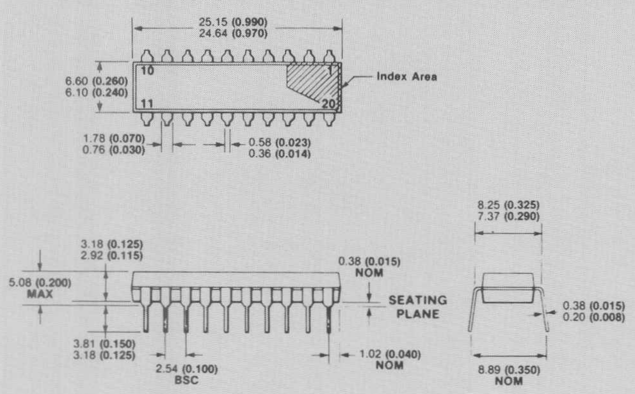
A Schlumberger Company



20 Lead Plastic Dual In-Line
Then, with the advent of the TTL logic family, the Plastic Dual In-Line package was devised—a package that had a much lower cost and was less fragile than the ceramic device. This plastic package soon became the industry standard, making digital ICs more usable than ever before.

20 Terminal Ceramic Leadless Chip Carrier

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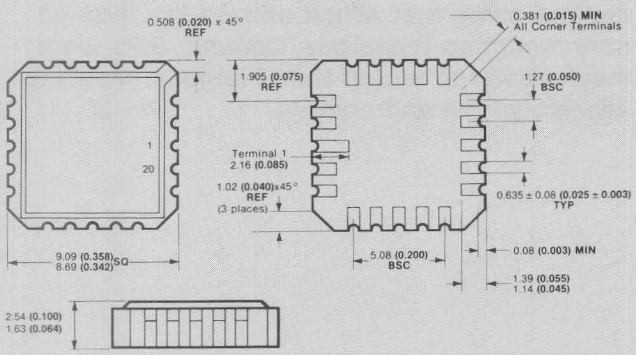
A Schlumberger Company



20 Lead Plastic Chip Carrier (PCC)

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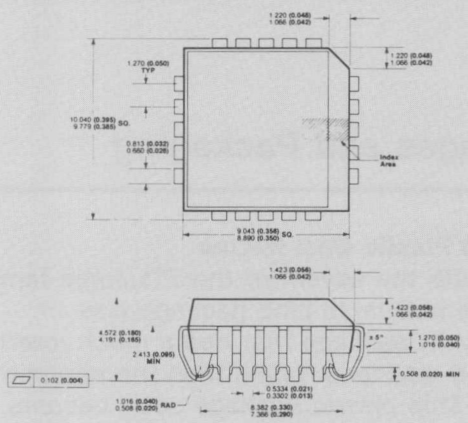
A Schlumberger Company



20 Lead Small Outline Integrated Circuit (SOIC)

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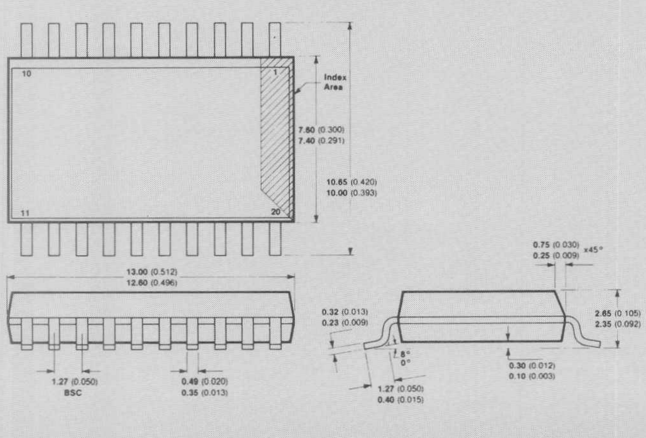
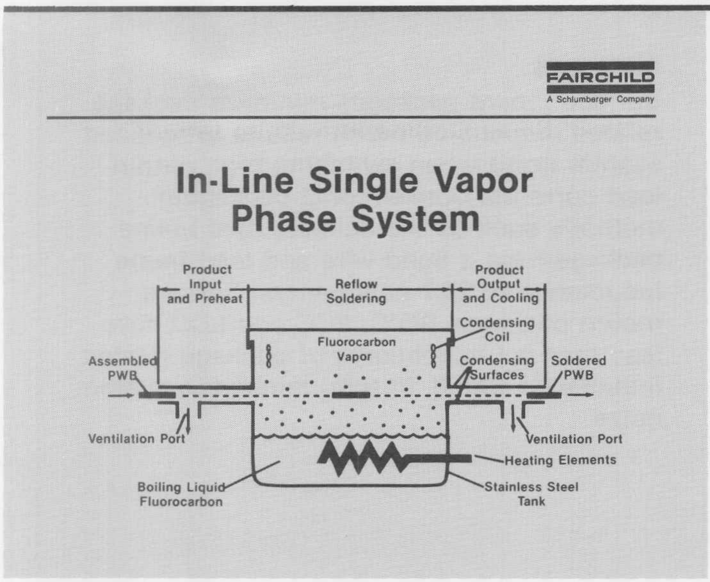


20 Terminal Ceramic Leadless Chip Carrier
20 Lead Plastic Chip Carrier
20 Lead Small Outline Integrated Circuit
Next came the development of surface mount devices—offering distinct advantages over the through hole devices. First, they are much faster to assemble. Typically, 20 times more surface mount devices can be assembled than through hole devices in a given period of time. Auto insert machines can assemble approximately 1000 units per hour compared to surface mount pick and place equipment which can assemble 5000 to 10,000 pieces.

Printed circuit boards for surface mount devices are also lower in cost. These boards, which offer higher chip packing density, have the potential for 6 times the functional complexity of a through hole dual in-line assembly.

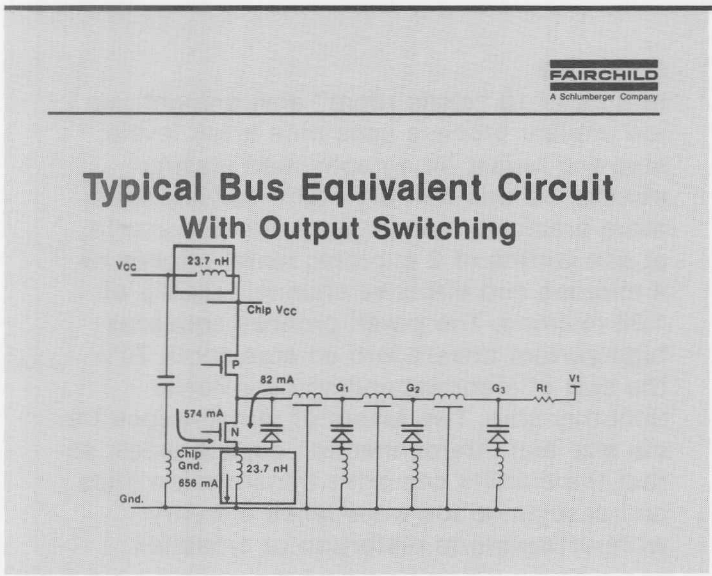
Surface mount devices include the Leadless Chip Carriers (LCC), the Plastic Chip Carriers (PCC), and the Small Outline Integrated Circuit (SOIC). All FACT devices are offered in these newer surface mount packages as well as the plastic and ceramic dual in-line designs.

Packages and Packaging



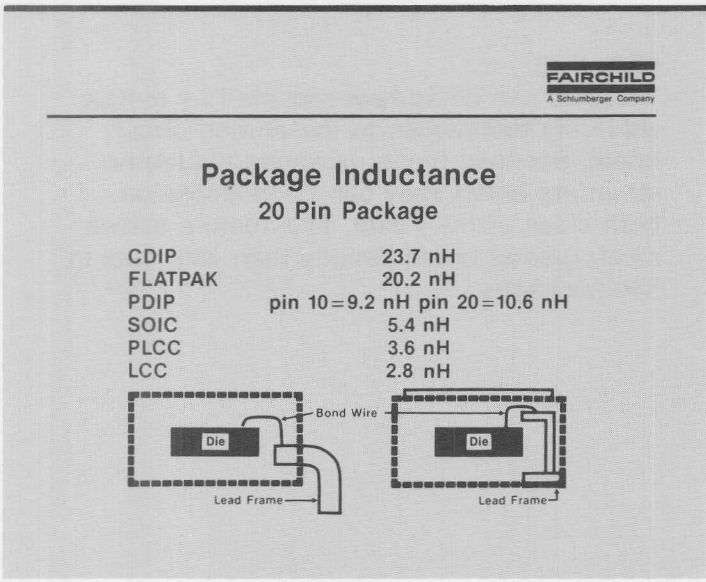
Slide 5.45
The LCC can be surface mounted by re-flow soldering techniques to the printed circuit board. Because these packages require no mounting holes, they can be mounted on both sides of the board. This feature allows much greater board density than with dual in-line packages.

Packages and Packaging



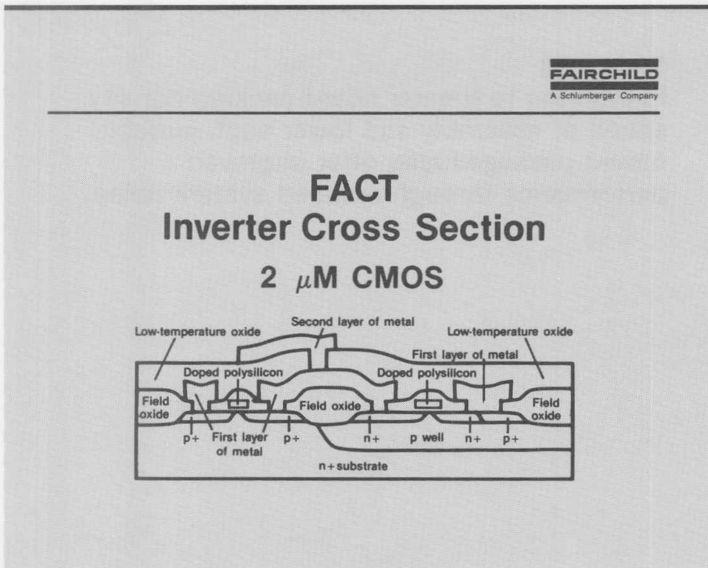
Slide 5.56
In addition to greater board packing density, speed of assembly and lower cost, surface mount packages also offer improved performance through reduced system noise.

Packages and Packaging



Slide 5.58
Surface mount packages minimize package related inductance which results in reduced system noise when switching high output load currents. Conventional packaging methods such as the ceramic dual in-line package have a bond wire and lead frame inductance of 23.7 nanohenrys. Surface mount packages SOIC, PCC and LCC have less than 5.4 nanohenrys of package related inductance which, in turn, minimizes system noise.

Packages and Packaging



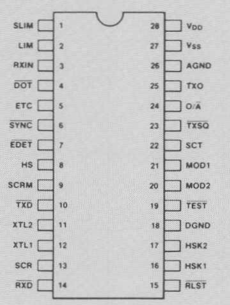
Slide 5.70
In a class 10 "clean room" environment, our ion implant process uses nine mask levels, step-and-repeat lithography, and plasma etching—a thin film dry etch—to yield finer, more predictable lines. Geometries come in at line widths of 2 microns, metal pitches of 4 microns and effective channel legnths of 1.25 microns. The p-well process squeezes high current drivers into an area about 70% the size of a corresponding Low Power Schottky chip. Two layers of metal reduce the die size and interconnection capacitances, so that the circuits can drive transmission lines and associated low-impedance circuitry without waveform distortion or crosstalk.

The near-planar surface of the second metal layer greatly improves reliability. The low resistance of the p-wells immunize the gates from latch-up, which is initiated through the substrate's parasitic structures. All gates in FACT devices can handle very high overload source and sink currents without latching up. FACT...the superior logic family...made possible only through advanced CMOS technology.

FAIRCHILD
A Schlumberger Company

Linear Division

μA212A
1200/300 bps Full Duplex Modem

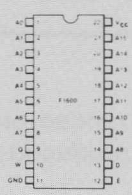


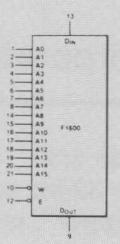
FAIRCHILD
A Schlumberger Company

Memory and High Speed Logic

F1600
65,536×1-Bit Static Random Access Memory

- Fast Access Time: 45nS/55nS/70nS (Maximum)
- Low Power Dissipation
- Directly TTL Compatible — All Inputs and Outputs
- Available in a 22-Pin DIP or LCC





Slides 5.79, 5.80
In our other divisions, Fairchild Semiconductor has also made a strong commitment to CMOS technology. In our Linear Division, we produce a modem chip which is the only single chip bell 212 compatible modem available. The Memory and High Speed Logic Division delivers the F1600 at 45 nanoseconds, 65K static RAMs, and high speed bipolar PALs.

Corporate Overview

Gate Array Division

FAIRCHILD
A Schlumberger Company

FGC Series
Advanced 2-Micron CMOS
Gate Array Family

- 500, 900, 1200, 1900, 2400, 3200, 4000, and 6000 Gates
- True 2-micron Silicon Gate CMOS Technology
- High Performance — Typical Internal Delays 1.1nS
- 8 mA Output Drive Current Standard
- Low Power Dissipation — Typically 20 μW/gate/MHz
- Selectable CMOS or TTL I/O
- Single 5V Power Supply
- Second Source — VLSI Technology, Inc.

Slide 5.81
The FGC6000 cell gate array in CMOS is available through our Gate Array Division.

Corporate Overview

Micrologic Division

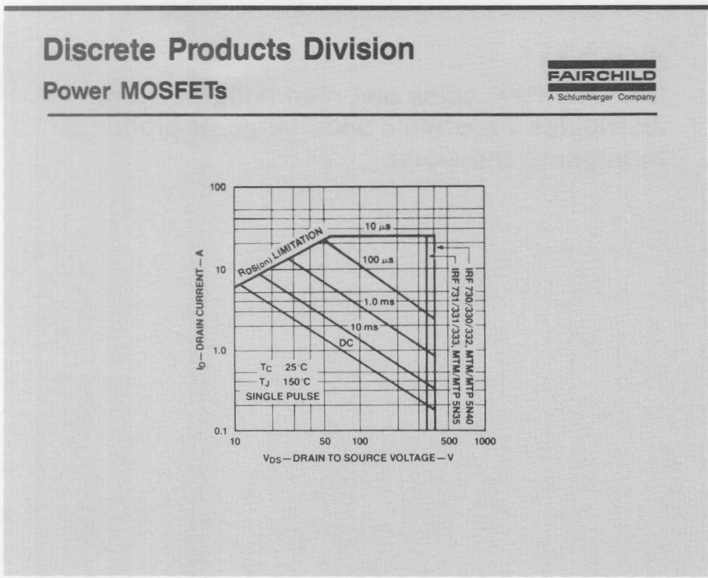
FAIRCHILD
A Schlumberger Company

Clipper Module

- 33 MHz Clock Frequency
- Simple Instructions Execute in 30nS
- 2 Separate 32-Bit Busses to Memory
- Integrated Floating Point Unit
- Coming Summer 1986

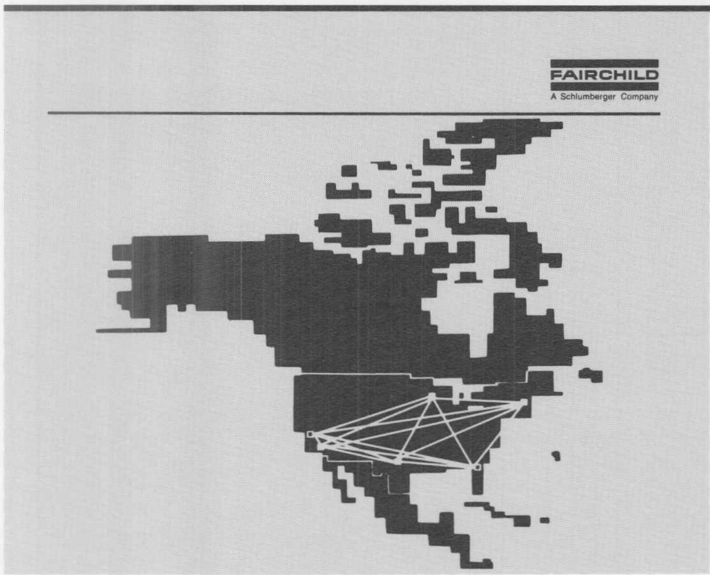
Slide 5.82
The 32-bit advanced processor, known as the "clipper", is produced in our Micrologic Division.

Corporate Overview



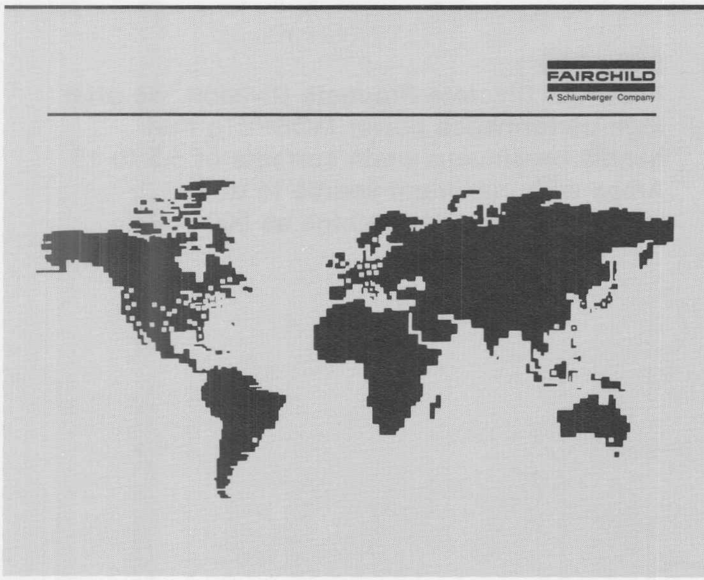
Slide 5.83
From our Discrete Products Division, we offer high performance power MOSFETs that handle continuous drain currents of 5.5 to 15 Amps with maximum source to drain breakdown voltages as high as 500 volts.

Corporate Overview



Slide 5.87
Through all these divisions, Fairchild supplies a complete line of CMOS technology products. Our Fairtech facilities, located in the high tech centers of the country, offer educational seminars and provide knowledgeable design assistance on all Fairchild products.

Corporate Overview



Slide 5.88
Our extensive sales and marketing network distributes Fairchild's wide range of products throughout the world.